CMT2189B User Guide

Overview

The CMT2189B is a low power, high performance, Flash-based, OOK RF transmitter chip embedded with the RISK MCU , which covers a wireless communication band of 240 - 960 MHz. The product is a part of the CMOSTEK NextGenRF™ product family which covers a complete product line consisting of transmitters, receivers, transceiver, etc.

The product models covered in this document are shown in the table below.

Table 1. Product Models Covered in This Document

Product Model	Frequency Range	Modulation Method	Tx Power	Tx Current	Configuration	Package
CMT2189B	240 - 960MHz	OOK	+13 dBm	17.5 mA	Embedded MCU	SOP14

Notes:

The test condition for the Tx power and Tx current is: 433.92 MHz, CW mode (always in the Tx carrier mode), Tx mode of Duty 50% and Tx current of 8.5 mA.

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1 Chip Architecture

1.1 Overall Operating Principle

The CMT2189B is a RF transmitting chip integrated with digital and analog parts altogether, which applies a crystal oscillator to provide the reference frequency and digital clock for PLL, supporting OOK modulation with a data rate range of 1 ~ 40 kbps. It supports status control through the MCU programming to fulfill various low power transmission applications.

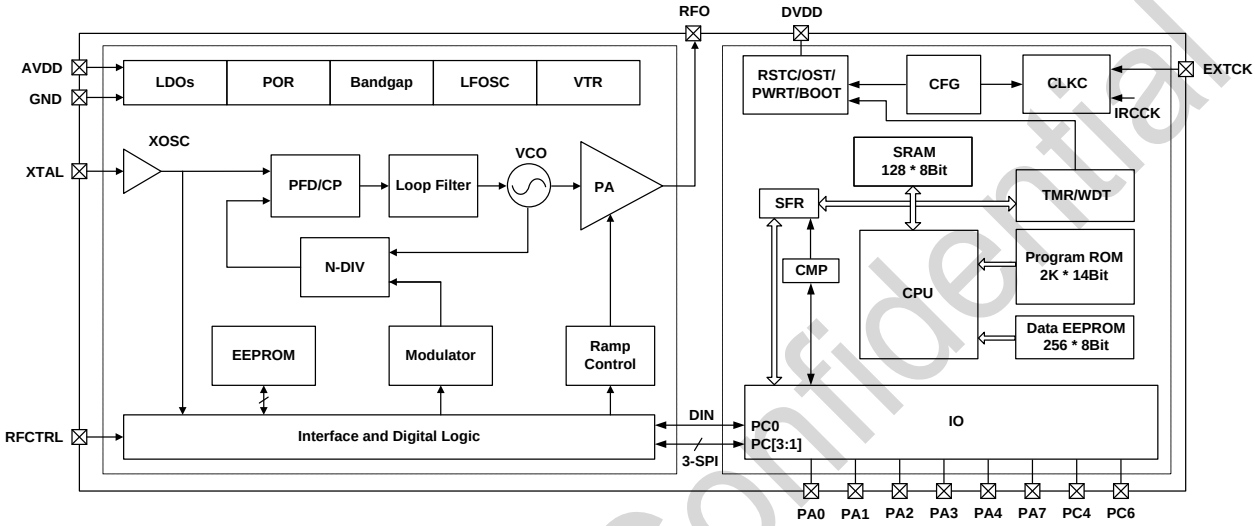


Figure 1. CMT2189B System Architecture

The chip adopts the PLL+PA architecture to achieve the Sub-GHz wireless transmission function with supports of FIFO packet mode and pass-through mode (in the FIFO packet mode, the embedded encoder allows users to select appropriate encoding formats). After the processed data is sent to the modulator (for the pass-through mode, data is not processed by the encoder but sent to the modulator directly after deburring), the modulator controls PLL and PA to have OOK modulation on the data and transmit the data after then.

By controlling the RF part through the 3-wire SPI interface, the MCU can control various status switching, mode selection and low power control.

1.2 IO Pin Description

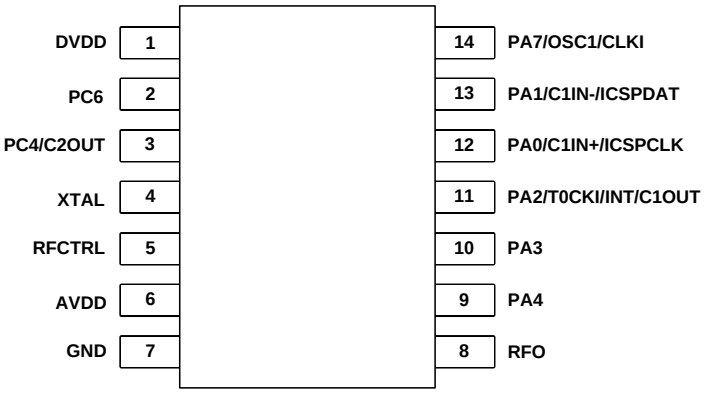


Figure 2. CMT2189B Pin Top View

Table 2. CMT2189B Pin Description - SOP14 Package

Pin #	Pin Name	Type	I/O	Description	
1	DVDD	Digital	I	Chip power supply +	
2	PC6	Digital	IO	General purpose IO	
3	PC4/C2OUT	Digital	IO	PC4	General purpose IO
				C2OUT	Comparator 2 output
4	XTAL	Analog	I	Crystal oscillator input in RF part	
5	RFCTRL	Digital	I	SPI interface enabling control in RF part, low active, internal pull up.	
6	AVDD	Analog	I	RF part power supply +	
7	GND	Digital	-	Chip power supply ground	
8	RF0	Analog	O	RF part PA output	
9	PA4	Digital	IO	General purpose IO with support of IOC and configurable pull-up	
10	PA3	Digital	IO	General purpose IO with support of IOC and configurable pull-up	
11	PA2/T0CKI/INT/C1OUT	Digital	IO	PA2	General purpose IO with support of IOC and configurable pull-up
				T0CKI	Timer 0 clock source input (Max=4MHz)
				INT	External interrupt input
				C1OUT	Comparator 1 output
12	PA0/C1IN+/ICSPCLK	Digital	IO	PA0	General purpose IO with support of IOC and configurable pull-up
				C1IN+	Comparator 1 input +
				ICSPCLK	Serial port clock signal for debug/programming mode
13	PA1/C1IN-/ICSPDAT	Digital	IO	PA1	General purpose IO with support of IOC and configurable pull-up
				C1IN-	Comparator 1 input -
				ICSPDAT	Serial port data signal for debug/programming mode
14	PA7/OSC1/CLKI	Digital	IO	PA7	General purpose IO with support of IOC and configurable pull-up
				OSC1	MCU crystal pin
				CLKI	External clock input pin
Internal pin	PC0/C2IN+/RFDIN	Digital	IO	PC0	General purpose IO
				C2IN+	Comparator 2 input +

Pin #	Pin Name	Type	I/O	Description	
				RFDIN	RF data input pin for pass-through mode
Internal pin	PC1/C2IN-/SDIO	Digital	IO	PC1	General purpose IO, connecting RF part and chip internally
				C2IN-	Comparator 1 output -
				SDIO	3-wire SPI serial bus data SDIO in RF part, which is a bidirectional port without pull-up or pull-down resistors.
Internal pin	PC2/SCLK	Digital	IO	PC2	General purpose IO, connecting RF part and chip internally
				SCLK	3-wire SPI serial bus clock SCLK in RF part
Internal pin	PC3/CSB	Digital	IO	PC3	General purpose IO, connecting RF part and chip internally
				CSB	3-wire SPI serial bus chip selection CSB in RF part with internal pull-up resistor

Notes:

1. The MCU has 2 built-in comparators, but the 2 internal comparators cannot be used due to the pin packaging limitation and the multiplexing of RF part for some pins. However the MCU still needs to have necessary comparator settings after initialization to avoid impact on other functions.

2. The clock source system of the MCU supports both internal oscillations and external oscillations. The external oscillation supports dual-end crystal and single-end clock source input. However, due to the package pin limitation, the PA6 has no package pin, therefore it does not support the external oscillation mode per dual-end crystal, namely only the external oscillation mode per single-end clock source is supported.

3. PC<3:0> is the internal control pin of the chip, which has no package pin, but it is used as a bus controlling RF part internally.

2 RF Part Configuration and Control Mechanism

2.1 Operating Mode

The built-in OOK Tx function of the CMT2189B supports 2 operating modes.

- Simple operating mode: the default entry mode upon power-up, namely, the non-configuration mode, which supports the pass-through Tx mode only.
- Advanced configuration mode: it supports register configuration and operating state control through the SPI bus, which supports both the FIFO and pass-through Tx mode.

Notes:

1. The pass-through Tx input sources in the 2 operating modes are different. Please see more details in below Sections.

2.2 Simple Operating Mode

In the simple operating mode, the only peripheral required is a crystal oscillator. Upon power-up, the chip controls data transmission through the internal PC1 (SDIO) to fulfill data transmission at the corresponding frequency. In this mode, the frequency multiplier factor is fixed to 16.5, calculated based on the following formula.

$$314\ \text{MHz} \leq F_{RF} \leq 480\ \text{MHz},$$

where FXTAL is the crystal frequency and FRF is the target frequency, and the frequency range is 314 MHz ~ 480MHz.

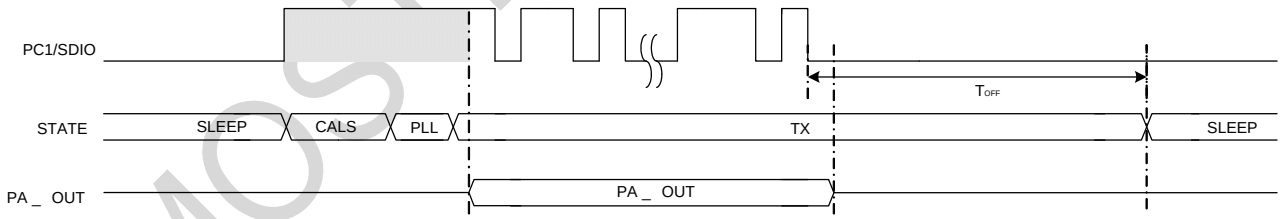


Figure 3. Tx Timing Diagram in the Simple operating Mode

Notes:

1. This mode supports a rate range of 1 ~ 20 kbps.
2. The maximum power output is fixed to +13 dBm. Users can reduce the Tx power by connecting a resistor to limit current before the chock inductor if it is needed.
3. The internal SPI bus does not need to send any control commands and only needs to hold PC<3:0> in a high resistance input status (except PC1).
4. The RFCTRL pin can be suspended in this mode.

5. In this mode, the data transmitting pin is PC1 (SDIO), which is set to 0 in the low power state (the normal state). When data transmitting is needed, it triggers on the rising edge to enter data transmitting state. After transmitting, PC1 is set to 0 and lasts for more than 20 ms (T_{OFF} time), and RF exits from the Tx mode automatically to enter the low power state.
6. For this mode, in low power state, PC1/SDIO is set 0 to output and PC2/SCLK, PC3/CSB, and PC0/RFDIN are set to high resistance input.

2.3 Advanced Configuration Mode

To achieve higher performance and more functions such as the target operating frequency of 868MHz and chip automatic packet transmitting in transmission process, users need to use the advanced configuration mode with supports of the following features.

- Support more frequency multiplication factors to cover a frequency range of 240 ~ 960 MHz.
- By filling the FIFO and transmitting the message automatically (repeatedly, multiple times and periodically), it can release the MCU to do more work (In the pass-through mode, this process will take up MCU resource).
- Support more accurate Tx rates with the accuracy determined by crystal, which is excellent in accuracy (in the pass-through mode, the speed is controlled by the MCU software, and the accuracy depends on the software and the internal RC).
- Support voltage detection function inside RF, which offers simple power supply voltage detection and analysis judgment processing.
- Dynamical Tx power adjustment according to the power supply voltage to save power and prolong battery life.

In this mode, the chip internal MCU can have the RF mode control by operating registers through the 3-wire SPI (PC3/CSB, PC2/SCLK, PC1/SDIO) to fulfill the 2 Tx modes.

1. Hardware packet Tx mode, which fills FIFO through SPI (see Section 2.9 for details)

The contents that need to be transmitted are filled into specified registers, which are automatically transmitted according to the speed, coding mode, number of packets and packet interval, etc.(the data package format and other relevant information are detailed in Section 2.7).

2. Pass-through Tx mode using PC0/RFDIN as data pin (see Section 2.10 for details)

That is, the 1-Pin Tx mode, the data stream is generated by the MCU and output through the specified pin to fulfill the most elementary operating mode, namely *data pin in, antenna out*.

Notes:

1. The 2 Tx modes mentioned above are all in the advanced configuration mode, namely configuring and operating the chip through SPI.
2. In the advanced configuration mode, it is required to control RFCTRL through other pins, therefore the RFCTRL pin cannot be suspended.
3. The pass-through mode in the advanced configuration mode is similar to the pass-through mode in simple operating mode, namely they both control data transmitting through a data pin, however the data input sources are different. In simple operating mode, the Tx input pin is PC1/SDIO, while in the advanced configuration mode, it is changed to PC0/RFDIN because PC1/SDIO is used as the serial data line of SPI. With both using the register configuring method, the pass-through mode in advanced configuration mode can support more frequency selection and power selection than that in the simple operating mode.

2.4 SPI Interface Timing

The RF function inside the chip is controlled by a 3-wire SPI, and the corresponding relationship between SPI interface and the IO of the MCU is as follows.

Table 3. Relationship between SPI Bus and Control Port

3-wire SPI	MCU Control Port	Function
CSB	PC3	Bus chip selection enabling, low active, built-in pull-up.
SCLK	PC2	Bus clock line, triggering on the rising edge
SDIO	PC1	Bi-directional bus data

Notes

1. SDIO, a bi-directional port, is used for data input and output. Both the address and data part are transmitted starting from MSB.
2. When the RF part is accessed, RFCTRL is pulled down[*] to enable SPI serial port function, then the chip selection enabling (PC3/CSB) is pulled down and a R/W bit is sent followed by a 7-bit register address. After the chip selection enabling (PC3/CSB) is pulled down, it is necessary to wait for at least half a PC2 (SCLK) cycle to start sending R/W bit. After sending the falling edge of the last PC2 (SCLK), the chip must wait for at least half a SCLK cycle, and then pull the PC3 (CSB) high.
3. In the SPI read operation as shown in the below figure, please pay special consideration on PC1/SDIO, since SDIO is a bi-directional port, which will switch from the input state to the output state on the falling edge of the 8th clock (the dotted line in the middle of the figure below), and SDIO needs to switch from the output state to the input state before the falling edge of the 8th clock.

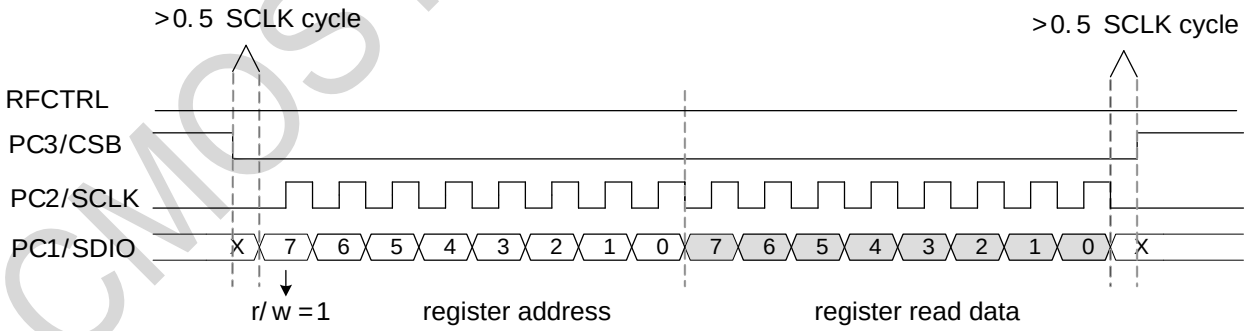


Figure 4. SPI Read Register Timing

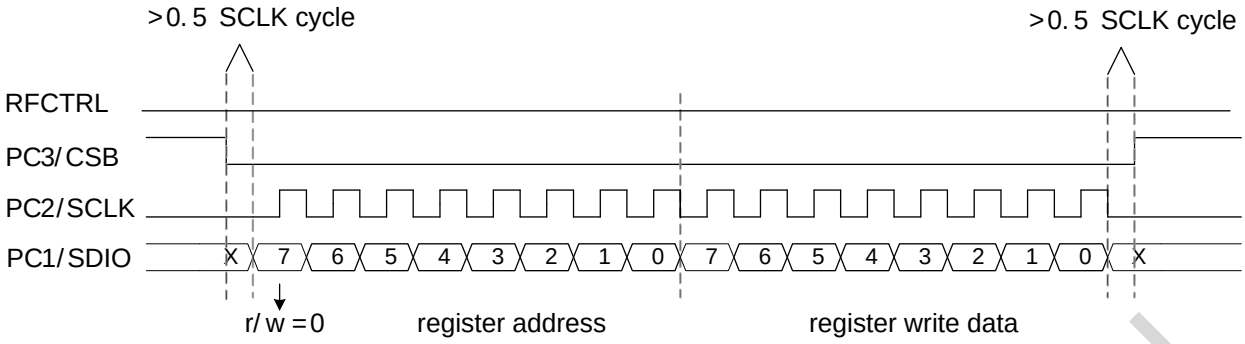


Figure 5. SPI Write Register Timing

Notes

1. RFCTRL is an input port requiring external control. It is recommended that users control it through any function port in the CMT2189B, and pull it down to enable SPI interface function. In the whole process, RFCTRL can keep low, but in the low power sleep mode, it needs to set the MCU pin controlling RFCTRL to a high impedance input, since the pull-up inside RFCTRL can pull the level high. Do not set the MCU pin to low output, since pull-down will consume power.

2.5 RF Configuration Parameter

When the CMT2189B operates in the advanced configuration mode, it can achieve a more wide operating frequency range, packet format, etc. These functions require corresponding configuration parameters, which can be exported by the RFPDK software. The operating process is: open the RFPDK software and select the CMT2157B model (it has the same specifications and performance with the built-in RF of the CMT2189B), as shown in the following figure.

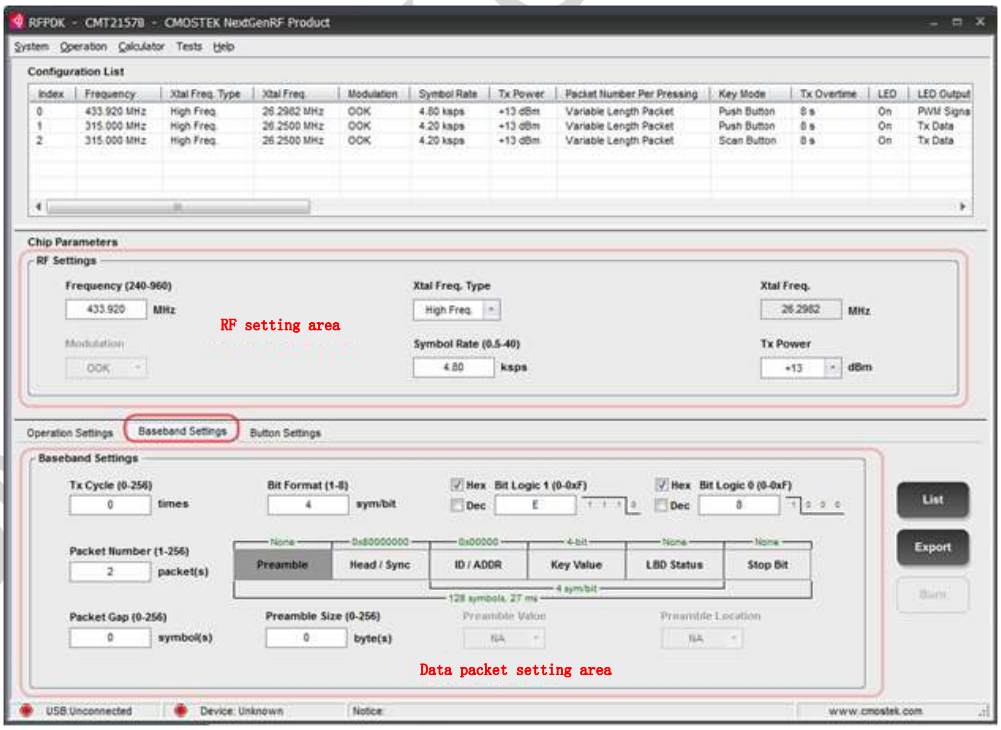


Figure 6. RFPDK Screen for CMT2157B

In the UI screen, there are mainly 2 areas: RF parameter settings area and data packet settings area. Users have configuration based on requirements according to the relevant registers described below, and then click *Export* to generate an exp file with file content as follows.

;--

; CMT2157B Configuration File

; Generated by CMOSTEK RFPDK 1.46

; 2017.11.14 13:47

;--

; (Among them, the annotation part with *;* is omitted.)

;--

; The following are the EEPROM contents

;--

0x7E4F

0x2134

0x017F

0x8015

0x0018

0x7F00

0x0000

0x8000

0x0000

0x0000

0xA073

0xE080

0x2010

0x8040

0x5030

0x6090

0xC0A0

0x0000

0x0100

0x027C

0x957B

0x70F0

0x0083

0x0000

;--

; The following is the CRC result for

; the above EEPROM contents

;--

0xEDFA

;--

; The following are for CMOSTEK

; use, customers can ignore them

;--

0x0000

0x0018

Among them, the specific configuration content is with red font, which are all 16-bit Word with a total of 24 Words contained, therefore users need to convert the 16-bit Word to the format of 8-bit register content. The conversion method is that the higher 8-bit of each 16-bit Word is an odd number address and the lower 8-bit is an even address. The conversion of 24 Words gets 48 register configuration values with an address range of 0x00 ~ 0x2E (the last 8-bit is invalid). According to the above file, the obtained register contents are as follows.

Table 4. Conversion Table from 16-bit EEPROM Word to 8-bits Register Content

16-Bit Word	Register Address	8-bit Register Configuration Value
0x7E4F	0x00	0x4F
	0x01	0x7E
0x2134	0x02	0x34
	0x03	0x21
0x017F	0x04	0x7F
	0x05	0x01
0x8015	0x06	0x15
	0x07	0x80
0x0018	0x08	0x18
	0x09	0x00
0x7F00	0x0A	0x00
	0x0B	0x7F
0x0000	0x0C	0x00
	0x0D	0x00
0x8000	0x0E	0x00
	0x0F	0x80

16-Bit Word	Register Address	8-bit Register Configuration Value
0x0000	0x10	0x00
	0x11	0x00
0x0000	0x12	0x00
	0x13	0x00
0xA073	0x14	0x73
	0x15	0xA0
0xE080	0x16	0x80
	0x17	0xE0
0x2010	0x18	0x10
	0x19	0x20
0x8040	0x1A	0x40
	0x1B	0x80
0x5030	0x1C	0x30
	0x1D	0x50
0x6090	0x1E	0x90
	0x1F	0x60
0xC0A0	0x20	0xA0
	0x21	0xC0
0x0000	0x22	0x00
	0x23	0x00
0x0100	0x24	0x00
	0x25	0x01
0x027C	0x26	0x7C
	0x27	0x02
0x957B	0x28	0x7B
	0x29	0x95
0x70F0	0x2A	0xF0
	0x2B	0x70
0x0083	0x2C	0x83
	0x2D	0x00
0x0000	0x2E	0x00

Users only need to write the above contents (as parameters) into the 0x01～0x2E register address while writing timing through SPI.

2.6 Configuration Register

The above exported configuration parameter address from 0x01 to 0x2E can be divided into three banks according to the functions, which are as follows:

Table 5. Configuration Register Area Partition Table

Bank	Address	Involved Content
Tx Bank	0x00 – 0x03	Tx frequency, Tx power
Packet Bank	0x04 – 0x27	Tx rate, packet format (only for hardware packet Tx mode）
System Bank	0x28 – 0x2E	System parameters

- **Tx Bank**

Tx bank parameter association is as follows.

The register address range is 0x00 ~ 0x03. These parameters are majorly about Tx central frequency and Tx power. When users need to transmit with multiple frequencies in applications, such as frequency hopping or adjusting Tx power according to voltage value, they can export different parameter tables after setting in the RFPDK, and it only need to take the segment in 0x00 ~ 0x03. The detailed register description is not discussed here.

- **Packet Bank**

The register address range associated with packet bank parameters is 0x04 ~ 0x27. These parameters are mainly setting items about hardware packet format, applicable to the hardware packet Tx mode only. Please refer to Chapter 2.7 for detailed register description.

- **System Bank**

The register address range associated with the system bank parameters is 0x28~0x2E. These parameters are the specific parameters for RF, not related to user applications. Users can configure them according to the parameters exported from RFPDK with no need to care about the details. Details will not be discussed here.

2.7 Packet Related Register

An overview of the packet bank register is shown in the below table.

Table 6. Packet Bank Register Overview

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	CUS_DIG1	SYMBOL_TIME<7:0>							
0x05	CUS_DIG2	SYMBOL_TIME<15:8>							
0x06	CUS_DIG3			LBD_TH<3:0>				LBD_OUT_EN	LBD_ON
0x07	CUS_DIG4					DEGLITCH_EN	TX_OVERTIMES<2:0>		
0x08	CUS_PKT1	TCYCLE_EN	INTERVAL_EN	STOP_EN	KEY_EN	SYNC_EN	PREAMBLE_LOCATION	PREAMBLE_SEL	PREAMBLE_EN
0x09	CUS_PKT2	TXCYCLE<7:0>							
0x0A	CUS_PKT3	PREAMBLE_LENGTH<7:0>							
0x0B	CUS_PKT4	KEY_LENGTH<2:0>				SYNC_LENGTH<4:0>			
0x0C	CUS_PKT5	SYNC_HEADER<7:0>							
0x0D	CUS_PKT6	SYNC_HEADER<15:8>							
0x0E	CUS_PKT7	SYNC_HEADER<23:16>							
0x0F	CUS_PKT8	SYNC_HEADER<31:24>							
0x10	CUS_PKT9	ADDR_ID<7:0>							

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x11	CUS_PKT10	ADDR_ID<15:8>							
0x12	CUS_PKT11	ADDR_ID<23:16>							
0x13	CUS_PKT12	ADDR_ID<31:24>							
0x14	CUS_PKT13	BIT_FORMAT<2:0>			ADDR_LENGTH<4:0>				
0x15	CUS_PKT14					STOP_LENGTH<3:0>			
0x16	CUS_PKT15	BIT_LOGIC_L<7:0>							
0x17	CUS_PKT16	BIT_LOGIC_H<7:0>							
0x18	CUS_PKT17	KEY<7:0>							
0x19 ~ 0x21	CUS_PKT18 ~ CUS_PKT26								
0x22	CUS_PKT27	STOP_BIT_L<7:0>							
0x23	CUS_PKT28	STOP_BIT_H<15:8>							
0x24	CUS_PKT29	INTERVAL_LENGTH<7:0>							
0x25	CUS_PKT30	PKT_NUM<7:0>							
0x26	CUS_RESV1								
0x27	CUS_RESV2							INTERVAL_STBY_DIS	STBY_PLLOFF_DIS

Notes

1. The gray area indicates it has content but users do not need to understand it. Users only need to configure them according to the parameters exported from RFPDK. Users need follow the procedure of *read-modify-write* to set an individual bit to 1 or 0.
2. The blue area indicates that users need to understand it. The registers will be detailed one by one in below.
3. The built-in packet structure pattern of the CMT2189B is the same as that of the CMT2157B. Users can select the packet structure of the CMT2157B in RFPDK configuration screen. The configuration parameters generated in *exp* are arranged according to required format and order. Users only need to fill in the specific data content during software executing.

2.7.1 Tx Rate

The Tx rate is determined by SYMBOL_TIME<15:0> and can be generated by RFPDK.

Table 7. Tx Rate Related Register

Register Name	Bits	R/W	Bit Name	Function description
CUS_DIG1 (0x04)	7:0	RW	SYMBOL_TIME<7:0>	Tx data rate of Packet format
CUS_DIG2 (0x05)	7:0	RW	SYMBOL_TIME<15:8>	

2.7.2 Hardware Packet Format

The CMT2189B supports hardware packet structure internally with data frame structure as follows.

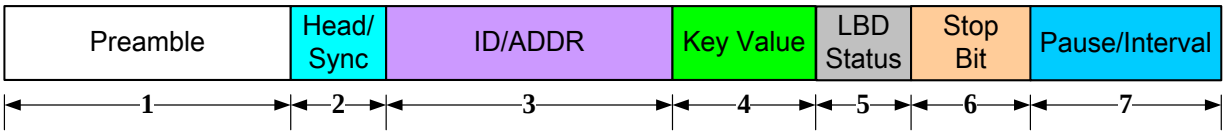


Figure 7. Packet Structure

As shown in the packet structure in the above figure, it contains 7 parts.

1. Preamble: optional, the value can be selected as 0x55 or 0xAA[1], ranging from 0 to 256 bytes (select any value within the range).
2. Head/Sync: synchronous word, optional, ranging from 0 to 32 bit[s][2] (select any value within the range).
3. ID/ADDR: sequence number, mandatory, ranging from 1 to 32 logic bits[3] (select any value within the range).
4. Key value: optional, ranging from 0 to 8 logic bits[3] (select any value within the range).
5. LBD status: low battery detection status bit, optional, occupying 1 logic bit [3];
6. Stop bit: optional, ranging from 0 ~ 16 bits[2] (select any value within the range).
7. Packet interval, fixed to send *0*, ranging from 0 ~ 256 bit[s][2];

Notes:

[1]. Preamble adopts NRZ format without encoding, e.g. for 0x55, the data flow is 0b01010101 at the set rate (0 represents low level and 1 represents high level).

[2]. Head/Sync, stop bit and pause/interval will not be encoded. They are output at the set rate just like the preamble code.

[3]. Logic bits, representing the encoded bits, which are described in detail below. Item 3 ~ 5 in the message structure as shown in the above figure all supports being encoded by the internal encoder.

For example, the coding rules choose at least 1 symbol as 1 logical bit, that is, 0b0 is logic 0, and 0b1 is logic 1 (NRZ encoding) with following settings.

Preamble: set to open. The value is 0xAA with a length of 5 bytes.

Head/Sync: set to open. The value is 0x2DD4 with a length is 2 bytes.

ID/ADDR: the value is 0x12345678 with a length of 4 bytes.

Key Value: the value is 0x9A.

LBD Status: set to close.

Stop bit: set to open. The value is 0xBCDE with a length of 16 bits (2 bytes).

Pause/interval: pause/interval: set to open. The length is 32 bits (4 bytes).

Then the data flow is as follows.

0xAA AA AA AA AA 2D D4 12 34 56 78 9A BC DE 00 00 00 00 AA AA AA AA AA 2D D4 12 34 56 78 9A BC DE 00…

2.7.3 Preamble

Table 8. Preamble Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	2	RW	PREAMBLE_LOCATION	When enabling Tcycle, it represents the preamble location in the packet structure of: 0: in one cycle, each packet contains 1 preamble, e.g. there are N packets in the 1 cycle, which contain N preambles. 1: in one cycle, it only contains 1 preamble, and it is in the first packet only. Note: the concept of Tcycle is described in detail later.
	1	RW	PREAMBLE_SEL	Preamble selection bit. 0: 0x55 1: 0xAA
	0	RW	PREAMBLE_EN	Preamble enabling bit. 0：Disable 1：Enable
CUS_PKT3 (0x0A)	7:0	RW	PREAMBLE_LENGTH<7:0>	The length of preamble can be configured to a value in 0~255. *0* represents that sending 1 byte of Preamble, and so on. 255 represents that it sends preamble with 256 bytes.

For users, if the PREAMBLE_EN is 0, a preamble is not sent, and if the configuration is 1, a preamble with 1 ~ 256 bytes is sent.

2.7.4 Head/Sync

Table 9. Head/Sync Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	3	RW	SYNC_EN	Sync enabling bit. 0: disable 1: enable
CUS_PKT4 (0x0B)	4:0	RW	SYNC_LENGTH<4:0>	The sync length can be configured as 0 ~ 31. 0 represents sending a sync with 1 symbol and so on. *31* represents sending a sync with *32* symbols. A symbol is random in length.
CUS_PKT5 (0x0C)	7:0	RW	SYNC_HEADER<7:0]>	The value of sync can be filled in different registers according to the different SYNC_LENGTH settings, please refer the next table for details.
CUS_PKT6 (0x0D)	7:0	RW	SYNC_HEADER<15:8>	
CUS_PKT7 (0x0E)	7:0	RW	SYNC_HEADER<23:16>	
CUS_PKT8	7:0	RW	SYNC_HEADER<31:24>	

(0x0F)				

Table 10. Relationship between Head/Sync Length Selection and Register

	SYNC/HEADER			
SYNC_LENGTH	<31:24>	<23:16>	<15:8>	<7:0>
0~7	√			
8~15	√	√		
16~23	√	√	√	
24~31	√	√	√	√

In the table, tick indicates a register to be filled. For example, if SYNC_LENGTH is set to 15, that is, the length is 16 symbols and sync value is 0x5678, then users will fill the value into SYNC_HEADER<31:24> and SYNC_HEADER<23:16> registers. MSB corresponds to the 31st bit and LSB corresponds to the 16th bit, that is, 0x56 is filled into SYNC_HEADER<31:24> and 0x78 is filled into SYNC_ HEADER<23:16>. For users, if the sync enabling bit is 0, a sync is not sent, and if the sync enabling bit is 1, a sync of 1-32 symbols is sent.

2.7.5 Addr/ID

Table 11. Addr/ID Related Registers

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT13 (0x14)	4:0	RW	ADDR_LENGTH<4:0>	The Addr ID length can be configured to 0 ~ 31. 0 represents sending an Addr of 1 logic bit, and so on. 31 represents sending an Addr of 32 logic bits.The logic bit length is random.
	7:5	RW	BIT_FORMAT<2:0>	The number of symbol that is contained by 1 logic bit can be configured to 0 ~ 7. 0 represents 1 symbol and so on. 7 represents 8 symbols.
CUS_PKT15 (0x16)	7:0	RW	BIT_LOGIC_L<7:0>	Logic 0 definition
CUS_PKT16 (0x17)	7:0	RW	BIT_LOGIC_H<7:0>	Logic 1definition
CUS_PKT9 (0x10)	7:0	RW	ADDR_ID<7:0>	Addr ID value
CUS_PKT10 (0x11)	7:0	RW	ADDR_ID<15:8>	
CUS_PKT11 (0x12)	7:0	RW	ADDR_ID<23:16>	
CUS_PKT12 (0x13)	7:0	RW	ADDR_ID<31:24>	

Table 12.Relationship between Addr/ID Length Selection and Register

	ADDR_ID			
ADDR_LENGTH	[31:24]	[23:16]	[15:8]	[7:0]
0~7	√			
8~15	√	√		
16~23	√	√	√	
24~31	√	√	√	√

In the table, tick indicates a register to be filled. For example, If ADDR_LENGTH is set to 15, the length is 16 logic bits and the value is 0x5678. Then users will fill the value into ADDR_ID<31:24> and ADDR_ID<23:16> registers. MSB is corresponding to the 31st bit and LSB corresponds to the 16th bit, that is, 0x56 is filled into ADDR_ID<31:24> and 0x78 is filled into ADDR_ID<23:16>.

Table 13. Relationship between Encoding Length Selection and Bit Enabling

	BIT_LOGIC_L/ BIT_LOGIC_H							
BIT_FORMAT	7	6	5	4	3	2	1	0
0	√							
1	√	√						
2	√	√	√					
3	√	√	√	√				
4	√	√	√	√	√			
5	√	√	√	√	√	√		
6	√	√	√	√	√	√	√	
7	√	√	√	√	√	√	√	√

In the table, tick indicates a register to be filled. For example, if BIT_FORMAT is set to 3, it represents 1 logic bit containing 4 symbols. If logic 0= 0b'1000', then users will fill the value into BIT_LOGIC_L<7:4>. If Logic 1= 0b'1110', then users will fill the value into BIT_LOGIC_H<7:4>. MSB corresponds to the 17th bit and LSB corresponds to the 14th bit.

Associating the above example, if ADDR_LENGTH is set to 20, ADDR_ID<31:12> is 0x56789, BIT_FORMAT is set to 4, BIT_LOGIC_L<7:4> is 0b '1000' and BIT_LOGIC_H<7:4> is 0b '1110'. Expand ADDR_ID as symbol, then the Tx data is as follows.

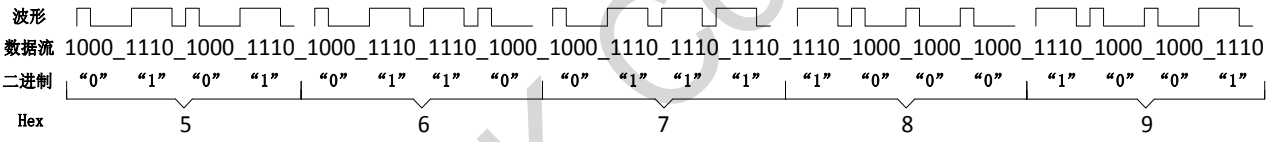


Figure 2-6. ADDR ID Example Diagram

That is, ID/ADDR = 0h '8E8E_8EE8_8EEE_E888_E88E', a total of 80 symbols, transmitted starting from the higher bit.

2.7.6 Key Value

Table 14. Key Value Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	4	RW	KEY_EN	Key enabling bit. 0: disable 1: enable
CUS_PKT4 (0x0B)	7:5	RW	KEY_LENGTH<2:0>	The key value length can be configured to 0~7. 0 represents sending a key of 1 logic bit, and so on. 7 represents sending a Key of 8 logic bits.The logic bit length is random.
CUS_PKT17 (0x18)	7:0	RW	KEY<7:0>	Key Value

The maximum length of the corresponding key value in the packet structure can be configured to 8, and the location of the tick in the table indicates the corresponding value of register to be filled. For example, if the KEY_LENGTH is set to 3, that is, the length is 4 logic bits and the value is 0x5, users will fill the value into KEY0<7:4>. For configuring logic bit as symbol, please refer to the description of Addr ID.

Table 15. Relationship between Key Value Length Selection and Bit Enabling

	KEY Value							
KEY_LENGTH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	√							
1	√	√						
2	√	√	√					
3	√	√	√	√				
4	√	√	√	√	√			
5	√	√	√	√	√	√		
6	√	√	√	√	√	√	√	
7	√	√	√	√	√	√	√	√

For users, if the KEY_EN is 0, the key value is not sent. If the configuration is 1, the key value of 1~ 8 logic bits is sent.

2.7.7 LBD Status Configuration

Table 16. LBD Status Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_DIG3 (0x06)	0	RW	LBD_ON	LBD (low battery detection) enabling bit. 0: disable 1: enable
	1	RW	LBD_OUT_EN	LBD output enabling bit（whether or not it is added to the message） 0: disable 1: enable
	5:2	RW	LBD_TH<3:0>	The voltage comparison threshold of the LBD. Iif the actual voltage is greater than the threshold, the LBD result is 1 (logic 1), and conversely, it is 0 (logic 0).
CUS_LBD_RESULT (0x4B)	3:0	R	LBD_RESULT<3:0>	Voltage measurement value

Notes

1. CUS_LBD_RESULT register is a functional register, which is not not a parameter exported through the RFPDK, see Section 2.8 for details.

2. The operating principle of LBD is: the chip compares the voltage value LBD_TH set by users (threshold of LBD) with the actual voltage value LBD_RESULT got by the test; if LBD_RESULT is smaller than LBD_TH, it indicates the low voltage occurs, on the contrary, it is the normal voltage. According to the comparison result, the LBD indicating signal will be output internally. If LBD_OUT_EN is configured as 1, the LBD result will be sent out as part of the packet. See Section 2.7.1 for details.

3. In the chip, the voltage value is converted by a 4-bit ADC to obtain LBD_RESULT with each step as 0.2 V. The relationship between the voltage value and LBD_RESULT is as follows.

Table 17. LBD_TH Configuration Register

NUM	LBD_TH	LBD_TH<3:0> or LBD_RESULT<3:0>
1	<1.45 V	4'b0000
2	1.45 ~ 1.65 V	4'b0001
3	1.65 ~ 1.85 V	4'b0010
4	1.85 ~ 2.05 V	4'b0011
5	2.05 ~ 2.25 V	4'b0100
6	2.25 ~ 2.45 V	4'b0101
7	2.45 ~ 2.65 V	4'b0110
8	2.65 ~ 2.85 V	4'b0111
9	2.85 ~ 3.05 V	4'b1000
10	3.05 ~ 3.25 V	4'b1001
11	3.25 ~ 3.45 V	4'b1010
12	3.45 ~ 3.65 V	4'b1011
13	3.65 ~ 3.85 V	4'b1100
≥14	>3.85	4'b1101

Notes

1. LBD is not tested in real time, but is tested once after PLL frequency calibration. Therefore users need to switch to STBY status first and then switch to Tx status to trigger the measurement process.
2. LBD_RESULT can be used as a condition for judgment. Therefore users can use LBD_RESULT as a quantitative analysis after triggering the LBD condition.

2.7.8 Stop Bit Configuration

Table 18. Stop Bit Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	5	RW	STOP_EN	Stop bit enabling bit. 0: disable 1: enable
CUS_PKT14 (0x15)	3:0	RW	STOP_LENGTH<3:0>	The stop bit length can be configured to 0 ~ 15. 0 represents sending a stop of 1 Symbol, and so on. 15 represents sending a stop of16 symbols, The symbol length is random.
CUS_PKT27 (0x22)	7:0	RW	STOP_BIT<7:0>	STOP_BIT Value
CUS_PKT28 (0x23)	7:0	RW	STOP_BIT<15:8>	

Table 19. Relationship between Stop Bit Length Selection and Bit Enabling

	STOP_BIT	
STOP_LENGTH	<15:8>	<7:0>
0~7	√	
8~15	√	√

In the table, tick indicates a register to be filled. For example, if STOP_LENGTH is set to 7, that is, the length is 8 symbols, and the value is 0x56. Then users will fill this value into STOP_BIT[15:8]. MSB corresponds to the 15th bit, and LSB corresponds to the 18th bit.

For users, if STOP_EN is configured to 0, stop bits are not sent. If it is configured to 1, stop bits with 1-8 symbols are sent.

2.7.9 Pause/Interval Configuration

Table 20. Pause/Interval Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	6	RW	INTERVAL_EN	Interval enabling bit. 0: disable 1: enable
CUS_PKT29 (0x24)	7:0	RW	INTERVAL_LENGTH<7:0>	The Interval length can be configured to 0 ~ 255. 0 represents sending 0 of 1 symbol, and so on, 255 represents sending 0 of 256 symbols.The Symbol length is random. Note that interval is fixed to sending 0.

Notes

1. In a strict sense, pause/interval is not an effective part of the packet structure, namely, it only sends a number of symbols of 0.
2. For users, if INTERVAL_EN is configured to 0, pause/interval is not sent. If it is configured to 1, a pause/interval with 1 ~ 256 symbols is sent.

2.7.10 Tcycle Configuration

Tcycle refers to a transmission cycle (transmission process) in hardware packet Tx mode. A transmission cycle can contain several (N) repeated packet transmissions with the support of pause/interval between packets. It also supports transmitting m data groups in a transmission cycle with each data group composed of N packets. The different transmission cycle configurations are shown in the below figure.

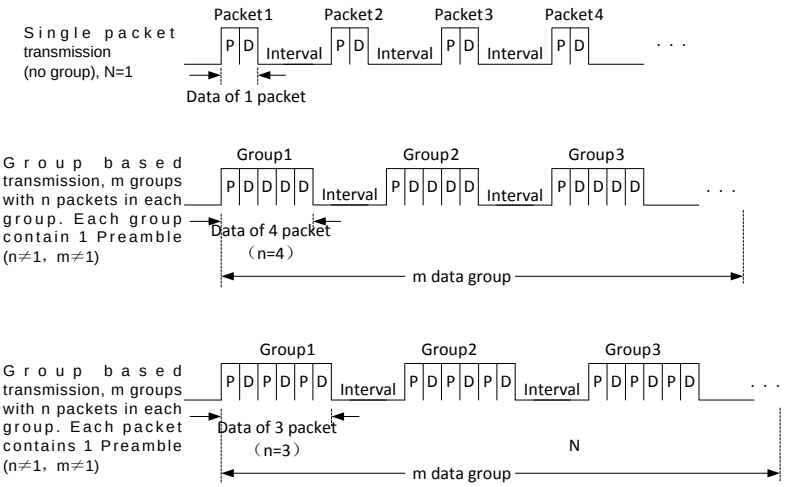


Figure 8. Various Packet Transmission Methods

- If Tcycle is disabled, the packet transmission follows the first method as shown in the above figure. If preamble is enabled, the preamble is fixed at the beginning of each packet.
- If both Tcycle and preamble are enabled and PREAMBLE_LOCATION = 1, the packet transmission follows the second method as shown in the above figure. That is, a preamble appears once in a group locating at the beginning of each group and preamble appears M times (M = TXCYCLE) within one transmission cycle.
- If Both Tcycle and preamble are enabled, and PREAMBLE_LOCATION = 0, the packet transmission follows the third method as shown in the above figure. That is, a preamble appears once in a group locating at the beginning of each group and preamble appears m*n (TXCYCLE * PKT_NUM) within one transmission cycle.

Notes

1. In the above figure, P = Preamble，D = Sync/Head + Addr/ID + Key Value + LBD Status + Stop Bit.
2. If Preamble is disabled, preamble is not sent.
3. If Interval is disabled, interval is not sent.
4. If Tcycle is disabled, preamble_location is configured to 0.
5. If Tcycle is disabled, Tcycle is configured to 0.

Table 21. Tcycle Configuration Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT1 (0x08)	2	RW	PREAMBLE_LOCATION	When Tcycle is enabled, it is the location of Preamble in the packet structure. 0: In one cycle, each Packet contains 1 Preamble, i.e. in one cycle, N Packets contain N Preambles. 1: In one cycle, only 1 Preamble is included, which is only in the first Packet.
	7	RW	TCYCLE_EN	Tcycle Enable bit: 0：Disable 1：Enable

Register Name	Bits	R/W	Bit Name	Function Description
CUS_PKT2 (0x09)	7:0	RW	TXCYCLE[7:0]	The number of Tcycle in one transmission cycle: 0-255 means sending 1-256 Tcycles.
CUS_PKT30 (0x25)	7:0	RW	PKT_NUM[7:0]	The number of Packet in one cycle: 0-255 means sending 1-256 Packets

2.8 State and Function Register

Table 22. State and Function Register Overview Table

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2F	CUS_SOFTRST	0xFF							
0x33	CUS_MODE					STBY		TX	SLEEP
0x34	CUS_DATA					DATAIN_EN			
0x4B	CUS_LBD_RESULT					LBD_RESULT			
0x4D	CUS_STATUS					MAIN_STATUS			

The above state and function registers cannot be exported in RFPDK. However users need to use these registers in advanced configuration mode, which involves chip state switching, state reading, reset, etc.

2.8.1 Soft Reset

0xFF is written to CUS_SOFTRST (0x2F) through the SPI bus, which can fulfill the RF part reset processing.

Table 23. Soft Reset Register

Control Register	Command Type	Command	Writing Value	Function Description
CUS_SOFTRST （0x2F）	Soft reset	soft_rst	0xFF	Reset the chip and allow the chip to perform initialization again and return to the SLEEP status.

Notes

1. After the soft_rst execution, the chip is reset again and users need to update configuration registers again according to requirements.
2. After power-up, configuration registers adopt internal default value (namely the EERPOM value programmed in factory) before the configuration register (CFG) is configured.

2.8.2 Operating State and State Switching

The CMT2189B RF supports 3 major operating states. In advanced configuration mode, the states and state switching are shown in the below diagram.

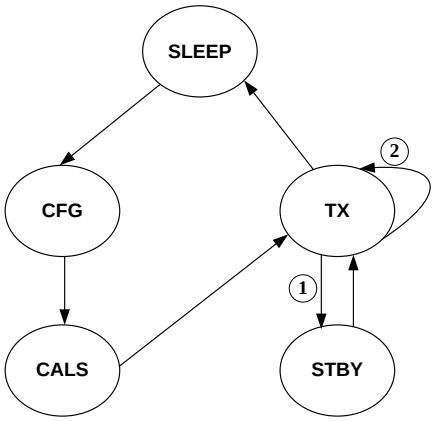


Figure 9. RF Operating States and State Switching

Table 24. State Description

Status/Process	Description
SLEEP	Low power mode, close all modules.
CFG	Configuring register process.
CALS	Calibrating analog module.
TX	Transmitting packets with all modules in the transmitter open.
STBY	Transmitting interval in the power saving mode. PA is turned off. PLL can be open according to configurations.The oscillator keeps running.

Notes

1. CFG refers to the process for configuring chip operating parameters through SPI for the MCU.
2. CALS refers to the process for calibrating the analog module in RF part internally. After transmitting is triggered, in RF part, the process is executed automatically and internally and it enters TX state when the processing completes.

Table 25. State Switching Command and Reset Command

Control Register	Command Type	Command	Writing Value	Function Description
CUS_MODE（0x33）	State jumping	go_sleep	0x01	Return SLEEP state
		go_tx	0x02	Enter TX state
		go_stby	0x08	Enter STBY state

2.8.3 Operating State Query

The user needs to query the current operating status by reading the CUS_STATUS (0x4D) status register, of which the lower 4-bit represents the current operating status. Details are listed in the below table.

Table 26. Operating Status Query Register

Status Register	State Coding	Description
CUS_STATUS （0x4D<3:0>）	0b0000	SLEEP
	0b1010	TX
	0b1101	STBY

2.9 Hardware Packet Tx Mode

2.9.1 Power-up Initialization

1. Upon chip power-up, it initializes ports and waits for 20 ms for stabilization.
2. Control RFCTRL=1.
3. Configure PC3/CSB, PC2/SCLK and PC0/RFDIN as high resistance input. Configure PC1/SDIO as output 0.
4. After initialization, the chip can enter low power based sleep state or perform other processing.

2.9.2 Tx Process

The CMT2189B hardware data packet frame structure is shown in the below figure. Please refer to Section 2.7.2 for the data frame structure descriptions.

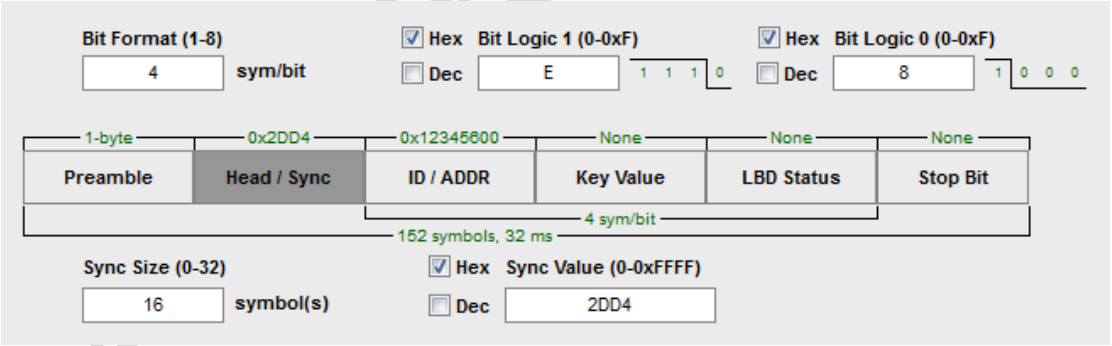


Figure 10. CMT2189B Hardware Packet Frame Structure

In this mode, the default value of *key value* is 0 and it cannot be changed by the software. Therefore, it is recommended to set the length of *key value* to *0* during configuration thus the corresponding key value will not appear in the packet. On the other hand, it is recommended to use the lowest byte ADDR_ID<7:0> of ID/ADDR as the actual key value with a corresponding register address 0x10.

For example, if a hardware packet frame structure according to Figure 10 is set as follows:

Preamble: be enabled, and set the value as 0xAA and the length as 1 byte;

Head/Sync: be enabled and set the value as 0x2DD4 and the length as 2 bytes;

ID/ADDR: set he value as 0x12345600 and the length as 4 bytes;

Key value: set the value as 0 and the length as 0 bit;

LBD Status: be disabled;

Stop Bit: be disabled;

then the data stream is as below (it uses 1527 encoding and ADDR_ID<7:0> is written to 0x88 as the key value):

0xAA 2D D4 888E 88E8 88EE 8E88 8E8E 8EE8 E888 E888

Hardware packets transmission should follow the below process.

1. Control RFCTRL=0, enable the SPI interface of the RF part and send the soft_rst command immediately. Then wait for 20 ms for stabilization to ensure the chip soft reset is completed.
2. Send the go_stby command through SPI and read the current status to confirm that the RF is in the standby state (it is recommended to wait for 2 ms after sending the command).
3. Configure related registers (transmission area, data packet format, etc., with a configuration range of 0x00 ~ 0x2E) according to user requirements.
   a) Configure all parameters derived from RFPDK in sequence.
   b) If necessary, modify individual registers (for example, write 0x88 to ADDR_ID<7:0> as the key value).
4. Set register 0x34<5> to 0, then set register 0x2A<1:0> to 0'b00.
5. Send the go_tx command through SPI, and start the chip to transmit the hardware data packet according to the above configuration.
6. After entering the TX state, the chip will transmit a certain number of data packets with the specific packet number configured in packet number on RFPDK (the maximum packet number is 256). The chip will enter the sleep mode automatically after the transmission ends. If to end an ongoing transmission, users can send the go_sleep command to let the chip enter the sleep mode, namely, the whole chip enters a low-power state.
7. After the transmission is completed, RFCTRL should be set to 1, and SPI and RFDIN should be switched to high-impedance input (SPI and RFDIN with internal pull-up). The MCU will enter the sleep state thereafter, namely, the whole chip enters a low-power state.

Notes

1. When transmission starts up again, execute the transmission process again.
2. In the 4th step, users need to follow the read-modify-write method to avoid modifying other bit values by mistake.
3. The standby state cannot be judged by transmission completion since it's in standby state as well during the data packet interval.
4. It should be noted that the internal pin state processing after transmission completion is different from the processing after power-up initialization.

2.10 Pass-through Tx Mode (Advanced Configuration Mode)

2.10.1 Power-up initialization

1. Upon chip power-up, it initializes ports and wait for 20 ms for stabilization.
2. Control RFCTRL = 1.
3. Configure PC3/CSB, PC2/SCLK and PC0/RFDIN as high resistance input. Configure PC1/SDIO as output 0.
4. After initialization, the chip can enter low power based sleep state or perform other processing.

2.10.2 Tx Process

To implement the pass-through transmission in configuration mode, users need to follow the process below.

1. Set PC0/RFDIN to 0 output.
2. Control RFCTRL = 0. Enable the SPI interface of RF part. Send the command soft_rst and wait for 20 ms for stabilization.
3. Set the register 0x34<3> to 1 and confirm the modification succeeds.
4. Send the command go_stby through SPI and confirm RF is in the standby state (it is recommended to wait for 2 ms after sending the command).
5. Configure the related registers according to user requirements (configuration range is 0x00~0x03).
6. Set the register 0x34<5> to 0, and then set the register 0x2A<1:0> to 0b01.
7. Send the command go_tx through SPI, and start the chip transmission according to above configurations (it is recommended to wait for 1 ms after sending the command).
8. Control PC0/RFDIN to transmit the required data stream.
9. After transmission completes, keep PC0/RFDIN to output 0.
10. Set the register 0x02<6:0> to 0 and set the register 0x4E<7> to 1.
11. Set the register 0x34<3> to 0 and confirm the modification succeeds.
12. Send the command go_sleep through SPI and enter sleep state.
13. Set the MCU pin that controls the RFCTRL to high resistance input. Switch PC3/CSB, PC2/SCLK and PC0/RFDIN to high resistance input (internal pull-up). Switch PC1/SDIO to output 0. Then the MCU will also enter the sleep mode, namely the whole device will enter the low power state.

Notes

1. In the 5th step, it only needs to configure 0x00 ~ 0x03 to adjust Tx frequency and Tx power. Other register configurations can be ignored.
2. When the transmission is started up again, execute the Tx process once again.
3. In step 3, 6, 1, 11, users need to use *read-modify-write* method to avoid modifying the value of other bits by mistake.

2.10.3 Related Register

Table 27. Pass-through Mode Related Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_DIG4 (0x07)	2:0	RW	TX_OVERTIMES[2:0]	The Tx ending overtime can be configured to 0~7. The calculation formula for overtime is: T = 20 ms + TX_OVERTIMES * 10 ms The overtime ranges from 20 ms to 90 ms.
CUS_DATA (0x34)	3	RW	DATAIN_EN	Data Input Enabling bit for RFDIN Tx mode. 0: disable 1: enable

In the pass-though mode, the data transmitting rate is controlled by RFDIN (PC0). When PC0 keeps output 0 for more than the time set in TX_OVERTIMES, it will enter the overtime exit mechanism automatically, namely it stops the current transmitting until the next triggering on the rising edge of PC0. Users need to consider the TX_OVERTIMES setting according to the encoding format. TX_OVERTIMES is set to 20 ms by default, and can increase to 90 ms by the step of 10 ms.

3 Program Memory

The 13-bit program address register can access up to 8 kbytes space (0x0000~0x1FFF). However the actual chip memory is 2 k Words, plus 4 additional user configuration banks (UCFGx) and factory configuration banks (FCFGx), therefore the total space is 64 k Words, which are all EEPROM. Among them, 0 ~ 0x7FF is the main program bank and 0x800 ~ 0x1FFF is the reserved bank which is not implemented. User and factory configuration information bank is 0x2000 ~ 0x203F.

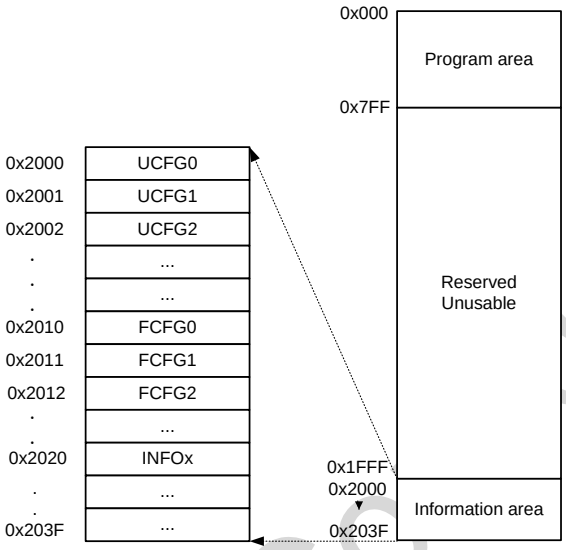


Figure 11. Program Space Address Mapping

4 Special Function Register(SFR)

4.1 Address Mapping

4.1.1 Bank0 SFR

Table 28. Bank0 Register List

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
0	INDF	Access the data memory using the content of FSR (non physical registers)								xxxx xxxx
1	TMR0	Timer0<7:0>								xxxx xxxx
2	PCL	Program counter<7:0>								0000 0000
3	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
4	FSR	Indirect data memory address pointer								
5	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00x0 0000
6										---- ----
7	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	0000 0000
8										---- ----
9										---- ----
A	PCLATH	-	-	-	Program counter<13:8>					---0 0000
B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
C	PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-	00-0 000-
D										---- ----
E										---- ----
F										---- ----
10										---- ----
11	TMR2	Timer2<7:0>								0000 0000
12	T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000
13										---- ----
14										---- ----
15										---- ----
16										---- ----
17										---- ----
18	WDTCON	-	-	-	WDTPS<3:0>				SWDTEN	---0 1000
19	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>			0000 0000

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
1A	PR0	PR0<7:0>								1111 1111
1B	MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-	---0 -00-
1C	SOSCPPRL	SOSCPR<7:0>								1111 1111
1D	SOSCPRH	-	-	-	-	SOSCPR<11:8>				---- 1111
1E										---- ----
1F										---- ----
20-7F		Bank0's SRAM, which is the general purpose RAM of 96 bytes.								xxxx xxxx

4.1.2 BANK1 SFR

Table 29. Bank1 Register List

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
80	INDF	Access the data memory using the content of SFR (non physical registers)								xxxx xxxx
81	OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82	PCL	Program Counter<7:0>								0000 0000
83	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
84	FSR	Indirect data memory address pointer								
85	TRISA	TRISA<7:6>		PA5	TRISA<4:0>					11x1 1111
86										---- ----
87	TRISC	TRISC<7:0>								1111 1111
88										---- ----
89										---- ----
8A	PCLATH	-	-	-	Program Counter<13:8>					---0 0000
8B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
8C	PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-	00-0 000-
8D										---- ----
8E	PCON							/POR	/BOR	---- --qq
8F	OSCCON	LFMOD	IRCF<2:0>			OSTS	HTS	LTS	SCS	0101 x000
90										---- ----
91										0000 0000
92	PR2	PR2<7:0>, Timer2 period register								1111 1111
93										---- ----

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
94										---- ----
95	WPUA	WPUA<7:6>		-	WPUA<4:0>					11-1 1111
96	IOCA	IOCA<7:0>								---- ----
97										---- ----
98										---- ----
99	VRCON	VREN	-	VRR	-	VR<3:0>				0-0- 0000
9A	EEDAT	EEDAT<7:0>								0000 0000
9B	EEADR	EEADR<7:0>								0000 0000
9C	EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD	--00 x0-0
9D	EECON2	-	-	-	-	-	-	-	WR	---- ---0
9E										---- ----
9F										---- ----
A0-BF		Bank1's SRAM, which is the general purpose RAM of 32 bytes.								xxxx xxxx
C0-EF										---- ----
F0-FF		SRAM, access Bank0's 0x70 ~ 0x7F.								xxxx xxxx

Notes

1. INDF is not a physical register.
2. The gray part is not implemented yet, please do not access.
3. '-' indicates that it is not implemented yet. Please do not use or write 1 or to the unimplemented register bits. It may be used in subsequent chip upgrading.

4.1.3 TMR0 (Addr:0x01)

Table 4-3. TMR0 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMR0	Timer0<7:0>, counter result register							
Reset	X	X	X	X	X	X	X	X
Type	RW							

4.1.4 STATUS (Addr:0x03)

Table 30. STATUS Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	-	-	PAGE	/TF	/PF	Z	HC	C
Reset	-	-	0	1	1	X	X	X
Type	-	-	RW	R	R	RW	RW	RW

Table 31. STATUS Bit Function Description

Bit	Name	Function
7:6	-	No function, read as *0*.
5	PAGE	Register bank selection bit. 0 = BANK0（00h - 7Fh） 1 = BANK1（80h - FFh）
4	/TF	Time out status bit. 1 = POR, after power up and the execution of CLRWDT or SLEEP instruction. 0 = WDT time out.
3	/PF	Power down flag bit. 1 = after POR or CLRWDT instruction execution. 0 = sleep instruction execution.
2	Z	Zero flag bit. 1 = the result of arithmetic operation or logic operation is 0. 0 = the result of arithmetic operation or logic operation is not 0.
1	HC	Half-carrying/borrowing (ADDWF, ADDLW, SUBLW and SUBWF instruction). For borrowing, the polarity is reversed. 1 = bit 4 carrying/borrowing occurs in the calculation result. 0 = bit 4 carrying/borrowing does not occur in the calculation result.
0	C	Carrying/borrowing (ADDWF, ADDLW, SUBLW and SUBWF instruction). 1 = carrying/borrowing occurs in the calculation result. 0 = carrying/borrowing does not occur in the calculation result.

Table 32. Flags in Each Reset Status

/TF	/PF	Condition
1	1	Power on or low voltage reset
0	u	WDT reset
0	0	WDT wake-up
u	u	MCLR reset occurred during normal operation
1	0	MCLR reset in the sleep state

Notes

1. Like any other registers, state registers can be target registers for any instructions. If an instruction affecting the bits Z, HC or C uses a state register as the target register, the write operation on the 3 bits will be prohibited since these 3 bits are affected by logic results only, namely it is set to 1 or cleared to 0. Therefore, after the execution of an instruction using a state register as the target register, the status content may be different than intended.
2. It is suggested to change the status register using the BCR, BSR, SWAPR and STR instructions only.

4.1.5 PORTA (Addr:0x05)

Table 33. PORTA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset	X	X	X	X	X	X	X	X
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 34. PORTA Bit Function Description

Bit	Name	Function
7	PA7	PORTA7 data
6	PA6	PORTA6 data
5	PA5	PORTA5 only has input function. There is no corresponding output data register.
4	PA4	PORTA4 data
3	PA3	PORTA3 data
2	PA2	PORTA2 data
1	PA1	PORTA1 data
0	PA0	PORTA0 data

4.1.6 PORTC（Addr:0x07）

Table 35. PORTC Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Reset	X	X	X	X	X	X	X	X

Type	RW	RW	RW	RW	RW	RW	RW	RW

Table 36. PORTC Bit Function Description

Bit	Name	Function
7	PC7	PORTC7 data
6	PC6	PORTC6 data
5	PC5	PORTC5 data
4	PC4	PORTC4 data
3	PC3	PORTC3 data
2	PC2	PORTC2 data
1	PC1	PORTC1 data
0	PC0	PORTC0 data

4.1.7 INTCON (Addr:0x0B)

Table 37. INTCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Table 38. INTCON Bit Function Description

Bit	Name	Function
7	GIE	Global interrupt enabling bit. 1 = enable all enabled interrupts 0 = disable all interrupts
6	PEIE	Peripheral interrupt enabling bit. 1 = enable all enabled peripheral interrupts 0 = disable all peripheral interrupts
5	T0IE	Timer 0 overflow interrupt enabling bit. 1 = enable 0 = disable
4	INTE	PA2/INT external interrupt enabling bit. 1 = enable 0 = disable
3	PAIE	PORTA port change interrupt enabling bit. 1 = enable the PORTA<7:0> change interrupt 0 = disable the PORTA<7:0> change interrupt
2	T0IF	Timer 0 overflow interrupt flag bit 1 = Timer 0 overflow occurs (must be cleared by software) 0 = Timer 0 overflow does not occur

1	INTF	PA2/INT external interrupt flag bit. 1 = PA2/INT external interrupt occurs (must be cleared by software) 0 = PA2/INT external interrupt does not occur
0	PAIF	PORTA change interrupt flag bit. 1 = one or more ports of PORTA<7:0> have state change (must be cleared in software) 0 = none of the PORTA<7:0> has state change

4.1.8 PIR1 (Addr:0x0C)

Table 39. PIR1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-
Reset	0	0	-	0	0	0	0	-
Type	RW	RW	-	RW	RW	RW	RW	-

Table 40. PIR1 Bit Function Description

Bit	Name	Function
7	EEIF	EEPROM write operation interrupt flag bit. 1 = EE write operation completes (must be cleared in software) 0 = EE write operation does not complete
6	CKMEAIF	Interrupt flag bit for the operation of fast clock measuring slow clock 1 = the operation of fast clock measuring slow clock completes (must be cleared in software.) 0 = the operation of fast clock measuring slow clock does not complete
5	-	Reserved bit, cannot be written to 1
4	C2IF	Comparator 2 interrupt flag bit. 1 = comparator 2 output changes 0 = comparator2 output does not change
3	C1IF	Comparator 1 interrupt flag bit. 1 = comparator 1 output changes 0 = comparator 1 output does not change
2	OSFIF	Oscillator failure interrupt flag bit. 1 = system oscillator fails and clock input switches to INTOSC (must be cleared by software) 0 = system clock runs normally
1	TMR2IF	Timer 2 and PR2 compare matching interrupt flag bit. 1 = Timer 2 and PR2 matching occurs (must be cleared by software) 0 = Timer 2 and PR2 matching does not occur
0	-	Reserved bit, cannot be written to 1.

4.1.9 TMR2 (Addr:0x11)

Table 41. TMR2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMR2	TMR2<7:0>							
Reset	0000 0000							
Type	RW							

4.1.10 T2CON (Addr:0x12)

Table 42. T2CON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>	
Reset	-	0000				0	00	
Type	-	RW				RW	RW	

Table 43. T2CON Bit Function Description

Bit	Name	Function
7	-	Reserved-bit, read as 0.
6:3	TOUTPS<3:0>	Timer 2 output dividing ratio selection bits. 0000 = 1:1 post dividing ratio 0001 = 1:2 post dividing ratio 0010 = 1:3 post dividing ratio 0011 = 1:4 post dividing ratio 0100 = 1:5 post dividing ratio 0101 = 1:6 post dividing ratio 0110 = 1:7 post dividing ratio 0111 = 1:8 post dividing ratio 1000 = 1:9 post dividing ratio 1001 = 1:10 post dividing ratio 1010 = 1:11 post dividing ratio 1011 = 1:12 post dividing ratio 1100 = 1:13 post dividing ratio 1101 = 1:14 post dividing ratio 1110 = 1:15 post dividing ratio 1111 = 1:16 post dividing ratio
2	TMR2ON	Timer 2 on/off. 1 = Timer 2 is on 0 = Timer 2 is off
1:0	T2CKPS<1:0>	Timer 2 driving clock dividing ratio selection bits. 00 = 1:1 dividing ratio. 01 = 1:4 dividing ratio. 1x = 1:16 dividing ratio.

4.1.11 WDTCON (Addr:0x18)

Table 44. WDTCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	-	-	-	WDTPS<3:0>				SWDTEN
Reset	-	-	-	0	1	0	0	0
Type	-	-	-	RW	RW	RW	RW	RW

Table 45. WDTCON Bit Function Description

Bit	Name	Function
7:5	-	Reserved bits, read as 0
4:1	WDTPS<3:0>	Watchdog timer period selection bits. 0000 = 1:32 0001 = 1:64 0010 = 1:128 0011 = 1:256 0100 = 1:512 (reset value) 0101 = 1:1024 0110 = 1:2048 0111 = 1:4096 1000 = 1:8192 1001 = 1:16384 1010 = 1:32768 1011 = 1:65536 11xx = 1:65536
0	SWDTEN	Software based watchdog timer enabling or disabling. 1 = WDT is turned on 0 = WDT is turned off

4.1.12 CMCON0 (Addr:0x19)

Table 46. CMCON0 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>		
Reset	0	0	0	0	1	0	0	0
Type	R	R	RW	RW	RW	RW	RW	RW

Table 47. CMCON0 Bit Function Description

Bit	Name	Function
7	C2OUT	Comparator 2 output bit When C2INV = 0, 1: C2VIN+ ＞ C2VIN- 0: C2V IN+ ＜ C2VIN- When C2INV=1, 1: C2VIN+ ＜ C2VIN- 0: C2V IN+ ＞ C2VIN-
6	C1OUT	Comparator 1 output bit. When C1INV = 0, 1: C1VIN+ ＞ C1VIN- 0: C1V IN+ ＜ C1VIN- When C1INV = 1, 1: C1VIN+ ＜ C1VIN- 0: C1V IN+ ＞ C1VIN-
5	C2INV	Comparator 2 reverse output control bit. 0 = no reverse 1 = reverse
4	C1INV	Comparator 1 reverse output control bit. 0 = no reverse 1 = reverse
3	CIS	Comparator input switching bit When CM[2:0] = 010, 1 = C1IN+ connects to C1VIN+, C2IN+ connects to C2VIN+ 0 = C1IN- connects to C1VIN-，C2IN- connects to C2VIN- When CM[2:0] = 001, 1 = C1IN+ connects to C1VIN+ 0 = C1IN- connects to C1VIN-
2:0	CM<2:0>	Comparator mode selection bits 000 = The comparator is turned off, and the CxIN pin is the analog IO pin. 001 = 3 inputs multiplexed to 2 comparators 010 = 4 inputs multiplexed to 2 comparators 011 = 2 common reference comparators 100 = 2 independent comparators 101 = 1 independent comparator 110 = 2 common reference comparators with outputs 111 = the comparator is turned off, and the CxIN pin is the digital IO pin.

4.1.13PR0 (Addr:0x1A)

Table 48. PRO Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PR0	PR0<7:0>							
Reset	0xFF							
Type	RW							

Table 49. PR0 Function Description

Bit	Name	Function
7:0	PR0<7:0>	Timer 0 period (compare) register

4.1.14 MSCKCON (Addr:0x1B)

Table 50. MSCKCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-
Reset	-	-	-	0	-	0	0	-
Type	-	-	-	RW	-	RW	RW	-

Table 51. MSCKCON Bit Function Description

Bit	Name	Function
7:5	-	Reserved bits, cannot be written to 1.
4	SLVREN	LVR enabling at software level. 1. When LVREN is enabled in compiling option SLVREN = 1 means LVR is enabled in operating mode and automatically disabled in sleep mode. SLVREN = 0 means LVR is always enabled. 2. When LVREN is disabled in compiling option LVR is disabled regardless of SLVREN value.
3	-	Reserved bit, cannot be written as 1.
2	CKMAVG	The measurement average mode of measuring slow clock period using fast clock 1 = enable the average mode.(measure and accumulate 4 times automatically) 0 = disable the average mode.
1	CKCNTI	Measuring slow clock period using fast clock enabling bit 1 = enable measuring slow clock period using fast clock 0 = disable measuring slow clock period using fast clock. Notes: The bit will automatically return to 0 after the measurement is completed.
0	-	Reserved bit, cannot be written to 1.

4.1.15 SOSCPR (Addr:0x1C/0x1D)

Table 52. SOSCPRL Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SOSCPRL	SOSCPR<7:0>							
Reset	0xFF							
Type	RW							

Table 53. SOSCPRH Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SOSCPRH	-				SOSCPR<11:8>			
Reset	-				1111			
Type	-				RW			

Table 54. SOSCPR Function Description

Bit	Name	Function
11:0	SOSCPR<11:0>	oscillator period (unit: number of fast clock period) is used for slow clock measurement.

4.1.16 OPTION (Addr:0x81)

Table 55. OPTION Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS<2:0>		
Reset	1	1	1	1	1	111		
Type	RW	RW	RW	RW	RW	RW		

Table 56. OPTION Bit Function Description

Bit	Name	Function
7	/PAPU	PORTA pull-up enabling bit. 1 = PORTA pull-ups are disabled 0 = PORTA pull-ups are enabled by the latch values of individual ports.
6	INTEDG	External interrupt triggering edge selection bit. 1 = PA2/INT pin Interrupt triggered on the rising edge 0 = PA2/INT pin Interrupt triggered on the falling edge
5	T0CS	Timer 0 clock source selection bit 1 = select PA2/T0CKI 0 = select internal instruction cycle clock (FOSC/2)

<table>
<tr><td>4</td><td>T0SE</td><td>Timer 0 clock source edge selection.
1 = trigger count on the falling edge of PA2/T0CKI
0 = trigger count on the rising edge of PA2/T0CKI</td></tr>
<tr><td>3</td><td>PSA</td><td>Prescaler assignment bit
1 = prescaler is assigned to WDT
0 = prescaler is assigned to Timer 0 module</td></tr>
<tr><td>2:0</td><td>PS<2:0></td><td>Prescaler ratio selection bits
<table>
<tr><th>Value</th><th>Timer 0</th><th>WDT</th></tr>
<tr><td>000</td><td>1:2</td><td>1:1</td></tr>
<tr><td>001</td><td>1:4</td><td>1:2</td></tr>
<tr><td>010</td><td>1:8</td><td>1:4</td></tr>
<tr><td>011</td><td>1:16</td><td>1:8</td></tr>
<tr><td>100</td><td>1:32</td><td>1:16</td></tr>
<tr><td>101</td><td>1:64</td><td>1:32</td></tr>
<tr><td>110</td><td>1:128</td><td>1:64</td></tr>
<tr><td>111</td><td>1:256</td><td>1:128</td></tr>
</table></td></tr>
</table>

4.1.17 TRISA (Addr:0x85)

Table 57. TRISA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 58. TRISA Bit Function Description

Bit	Name	Function
7:6	TRISA<7:6>	PORTA<7:6> port direction control bits 1 = input 0 = output
5	TRISA<5>	PORTA5 port direction control bit. Input only, fixed to 1.
4:0	TRISA<4:0>	PORTA<4:0> port direction control bits. 1 = input 0 = output

4.1.18 TRISC (Addr:0x87)

Table 59. TRISC Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	R	RW	RW	RW	RW	RW

Table 60. TRISC Bit Function Description

Bit	Name	Function
7:0	TRISC<7:0>	PORTC<7:0> port direction control bits 1 = input 0 = output

4.1.19 PIE1（Addr:0x8C）

Table 61. PIE1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-
Reset	0	0	-	0	0	0	0	-
Type	RW	RW	-	RW	RW	RW	RW	-

Table 62. PIE1 Bit Function Description

Bit	Name	Function
7	EEIE	EEPROM write operation completion interrupt enabling bit. 1 = enable write operation completion interrupt 0 = disable write operation completion interrupt
6	CKMEAIE	Fast clock measuring slow clock operation completion interrupt enabling bit. 1 = enable fast clock measuring slow clock operation completion interrupt 0 = disable fast clock measuring slow clock operation completion interrupt
4	C2IE	Comparator 2 interrupt enabling bit 1 = enable the comparator 2 interrupt 0 = disable the comparator 2 interrupt
3	C1IE	Comparator 1 interrupt enabling bit. 1 = enable comparator 1 interrupt 0 = disable comparator 1 interrupt
2	OSFIE	Oscillator failure interrupt enabling bit. 1 = enable the oscillator failure interrupt 0 = disable the oscillator failure interrupt

1	TMR2IE	Timer 2 and PR2 compare matching interrupt enabling bit. 1 = enable 0 = disable

4.1.20 PCON（Addr:0x8E）

Table 63. PCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	-	-	-	-	-	-	/POR	/BOR
Reset	-	-	-	-	-	-	q	q
Type	-	-	-	-	-	-	RW	RW

Table 64. PCON Bit Function Description

Bit	Name	Function
1	/POR	Power-on reset flag, active low. 0 = power on reset occurs 1 = no power on reset occurs /POR is set to 0 after a power-on reset occurs. It should be set to 1 by the software after then.
0	/BOR	Brown-out reset flag, active low. 0 = brown-out reset occurs 1 = no brown-out reset occurs or it is set to 1 by software.

4.1.21 OSCCON (Addr:0x8F)

Table 65. OSCCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OSCCON	LFMOD	IRCF<2:0>			OSTS	HTS	LTS	SCS
Reset	0	101			1	0	0	0
Type	RW	RW			R	R	R	RW

Table 66. OSCCON Bit Function Description

Bit	Name	Function
7	LFMOD	Internal low frequency oscillation mode. 1 = 256 k oscillation frequency mode 0 = 32 k oscillation frequency mode
6:4	IRCF<2:0>	Internal oscillator frequency selection bits. 111 = 16 MHz 110 = 8 MHz 101 = 4 MHz(default) 100 = 2 MHz 011 = 1 MHz 010 = 500 kHz 001 = 250 kHz 000 = 32 kHz (LFINTOSC)
3	OSTS	Oscillator start-up timeout status bit. 1 = device is running from the external system clock defined by the FOSC<2:0>. 0 = device is running from the internal system clock
2	HTS	Internal high frequency clock status bit 1 = HFINTOSC is stable 0 = HFINTOSC is not stable yet
1	LTS	Internal low frequency clock status bit. 1 = LFINTOSC is stable 0 = LFINTOSC is not stable yet
0	SCS	System clock selection bit. 1 = select system clock as internal oscillator 0 = clock source is defined by FOSC<2:0>

4.1.22 PR2 (Addr:0x92)

Table 67. PR2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PR2	PR2<7:0>							
Reset	0xFF							
Type	RW							

Table 68. PR2 Bit Function Description

Bit	Name	Function
7:0	PR2<7:0>	Timer 2 period (compare) register (see Timer 2 specific sections for details).

4.1.23 WPUA (Addr:0x95)

Table 69. WPUA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WPUA	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
Reset	1	1	-	1	1	1	1	1
Type	RW	RW	-	RW	RW	RW	RW	RW

Table 70. WPUA Bit Function Description

Bit	Name	Function
7:6	WPUA<7:6>	PORTA weak pull-up enabling bit. 1 = enable 0 = disable
4:0	WPUA<4:0>	PORTA weak pull-up enabling bit. 1 = enable 0 = disable

4.1.24 IOCA (Addr:0x96)

Table 71. IOCA Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IOCA	IOCA<7:0>							
Reset	0x00							
Type	RW							

Table 72. IOCA Bit Function Description

Bit	Name	Function
7:0	IOCA<7:0>	PORTA port state triggered interrupt control bit. 1 = enable port state triggered interrupt 0 = disable port state triggered interrupt

4.1.25 VRCON (Addr:0x99)

Table 73. VRCON Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VRCON	VREN	-	VRR	-	VR<3:0>			
Reset	0	-	0	-	0			
Type	RW	-	RW	-	RW			

Table 74. VRCON Bit Function Description

Bit	Name	Function
7	VREN	CVref enabling bit 1 = CVref circuit runs 0 = CVref circuit powers down, no IDD drain
5	VRR	CVref range selection bit. 1 = low level range 0 = high level range
3:0	VR<4:0>	CVref value selection control bit. When VRR = 1, CVref = (VR<4:0>÷24) ×VDD When VRR = 0, CVref = (VDD÷4) + (VR<4:0>÷32)×VDD

4.1.26 EEDAT（Addr:0x9A）

Table 75. EEDAT Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EEDAT	EEDAT<7:0>							
Reset	0x00							
Type	RW							

4.1.27 EEADR（Addr:0x9B）

Table 76. EEADR Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EEADR	EEADR<7:0>							
Reset	0x00							
Type	RW							

4.1.28 EECON1（Addr:0x9C）

Table 77. EECON1 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD
Reset	-	-	0	0	X	0	-	0
Type	-	-	RW	RW	RW	RW	-	W

Table 78. EECON1 Bit Function Description

Bit	Name	Function
5,4,2	WREN<2:0>	Data EEPROM write operation enabling bit. 111 = enable programming EEPROM by software. Each bit will restore to 0 automatically after programming completes. Other values = disable programming EEPROM by the software
3	WRERR	Data EEPROM write operation error flag bit. 1 = write operation is terminated due to WDT or external reset occurring during the EEPROM programming period. 0 = write operation completes normally during the EEPROM programming period.
0	RD	Data EEPROM read operation control bit. The bit is write-only. It will return always 0 if it is read. 1 = initiate a data EEPROM read period 0 = does not initiate read

4.1.29 EECON2 (Addr:0x9D)

Table 79. EECON2 Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EECON2	-	-	-	-	-	-	-	WR
Reset	-	-	-	-	-	-	-	0
Type	-	-	-	-	-	-	-	RW

Table 80. EECON2 Bit Function Description

Bit	Name	Function
0	WR	Data EEPROM write operation control bit. Read operation, 1= Data EEPROM is in the programming period 0= Data EEPROM is not in the programming period Write operation, 1= initiates a data EEPROM programming period 0= does not provide the function

4.1.30 Configuration Register UCFGx

The software cannot access UCFG0, UCFG1 and UCFG2. They can only be written by the hardware (programming) in the power up process.

- **UCFG0, PROM address 0x2000**

Table 81. UCFG0 Configuration Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG0	-	CPB	MCLRE	PWRTEB	WDTE	FOSC<2:0>		

Table 82. UCFG0 Bit Function Description

Bit	Name	Function
6	CPB	1 = disable Flash content protection 0 = enable Flash content protection. It can be read by the MCU and series ports cannot read it. Notes: The bit can only be rewritten from 1 to 0, but it cannot be rewritten from 0 to 1. The only way to rewrite from 0 to 1 is to erase the registers including USER_OPT, then CPB will become1 after it powers up again.
5	MCLRE	1 = PA5/MCLR pin executes the MCLR function, which is a reset pin. 0 = PA5/MCLR pin executes the PA5 function, which is a digital input pin.
4	PWRTEB	1 = disable PWRT 0 = enable PWRT
3	WDTE	1 = enable WDT, the program cannot disable it. 0 = disable WDT, but the program can enable WDT by setting the SWDTEN bit of the WDTCON
2:0	FOSC<2:0>	000 = 32 k crystal oscillator mode. The PA6/PA7 connects the low frequency crystal oscillator. 001 = 20 MHz crystal oscillator mode. The PA6/PA7 connects the high speed crystal oscillator. 010 = external clock mode, the PA6 is an IO pin, the PA7 connects to the clock input. 011 = INTOSC mode. The PA6 outputs the system clock divided by 2. The PA7 is an IO pin. 1xx = INTOSCIO mode, both the PA6 and PA7 are IO pins

- **UCFG1, PROM address 0x2001**

Table 83. UCFG1 Configuration Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG1	-	-	TSEL	FCMEN	IESO	RD_CTRL	LVREN <1:0>	

Table 84. UCFG1 Bit Function Description

Bit	Name	Function
5	TSEL	Instruction cycle selection bit. 1 = the instruction cycle duration is 2T 0 = the instruction cycle duration is 4T
4	FCMEN	Clock fault monitoring enabling bit. 1 = enable the clock fault monitoring 0 = disable the clock fault monitoring
3	IESO	2-speed clock enabling bit. 1 = enable 0 = disable
2	RD_CTRL	Port read control bit in output mode 1 = read the value of the PAD returned from the data port 0 = read the value of the Latch returned from the data port

1:0	LVDEN<1:0>	Low voltage reset selection bit 00 = enable the low voltage reset Others = disable the low voltage reset

- **UCFG2, PROM address 0x2002**

Table 85. UCFG2 Configuration Register

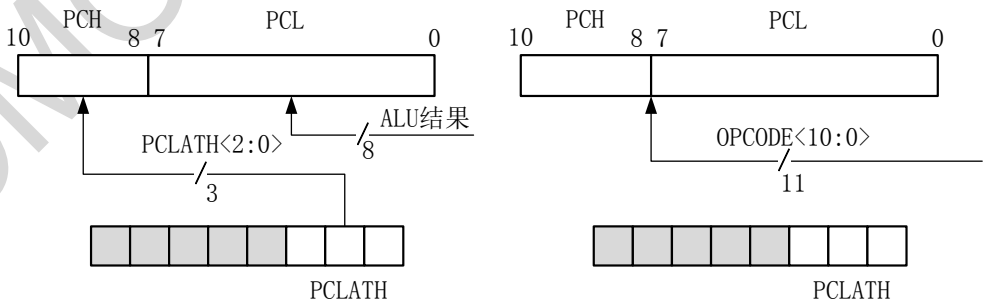
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UCFG2	-	-	-	-	LVDS<3:0>			

Table 86. UCFG2 Bit Function Description

Bit	Name	Function
7:4	-	Reserved bit
3:0	LVDS[3:0]	Low voltage reset threshold selection Value / Voltage 0010 / 1.8V 0011 / 2.0V 0100 / 2.2V 0110 / 2.8V Others / Reserved

4.1.31 PCL and PCLATH

The program counter (PC) is 11-bit. The lower 8 bits are from the PCL register, which are a readable and writable register. The higher 3 bits (PC<10:8>) are from the PCLATH, which cannot be read and written directly. Upon reset, the PC will be cleared to 0. The 2 situations for the PC loading are shown in the below figure. It should be notified that, for the LCALL and LJUMP instructions on the right side of the figure, PCLATH is not required since the operating code in the instructions is 11-bit, and the chip PC is exactly 11-bit.



Instruction with PCL as Instruction Target LJUMP and LCALL Instruction

Figure 12. PC Loading in Different Situations

Modify PCL

Any instruction execution with PCL as the target register will cause the program counter PC<10:8> bits to be replaced by the PCLATH register content. Therefore the entire contents of the program counter can be changed by writing the desired high 3 bits to the PCLATH register.

The LJUMP instruction calculation is achieved by adding an offset to the program counter (ADDWR PCL). Users should pay more consideration when need to jump into the look-up table or the program branch table (namely, calculate the LJUMP). Assuming that the PCLATH is set as the start address of the table and the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 within the table, the PCLATH must be increased by 1.

4.1.32 INDF and FSR Register

INDF is not a physical register, therefore addressing the INDF will cause an indirect addressing with an addressable address range of 0 ~ 255. Any instruction using the INDF register actually accesses the unit that the file selection register FSR points to. Reading the INDF indirectly will return 0. Writing the INDF indirectly will cause the control operation (It may affect the state flag bit).

5 System Clock Source

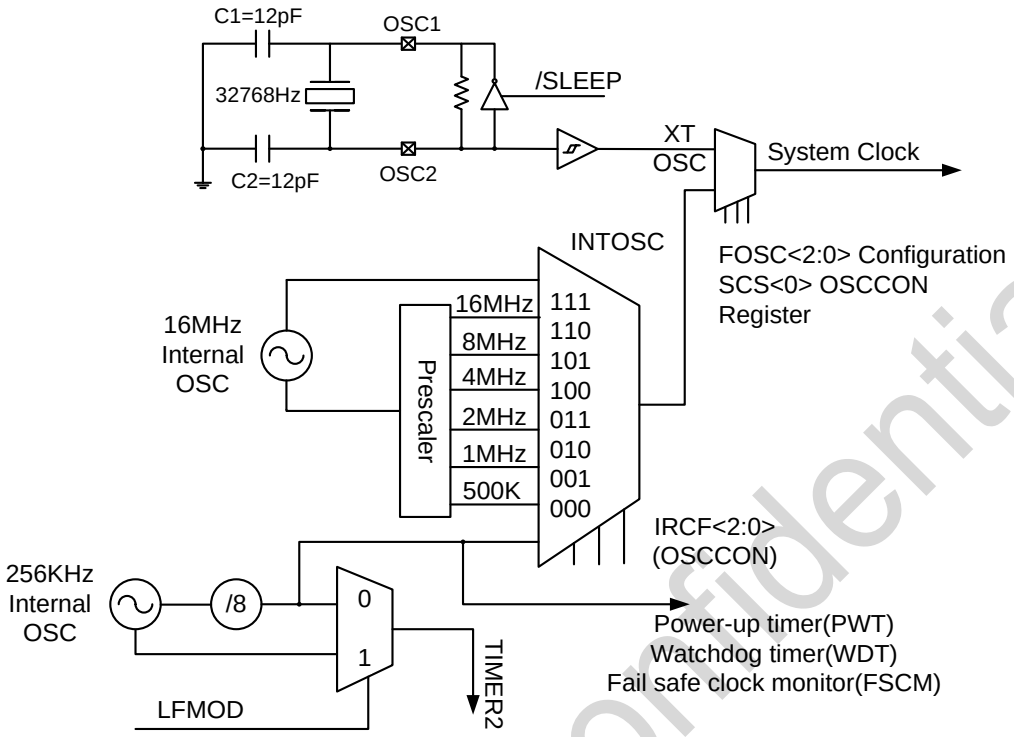


Figure 13. System Clock Source Diagram

The chip contains 3 clock sources: 2 built-in oscillators used as various clock sources, and 1 external clock input source. The built-in oscillator includes 1 internal 16 M high-frequency precise oscillator (HFINTOSC), and 1 internal 32 k/256 k low-frequency and low-power oscillator (LFINTOSC). These clocks or oscillators, combined with prescalers, can provide the system with a variety of frequency clock sources. The prescaler ratio of the system clock source can be controlled by the IRCF<2:0> bit in the OPTION register.

Notes:

1. The watchdog, system clock source (IRCF=000) and PWRT all use the output of frequency division by 8, that is 32 k Hz, regardless of the LFMOD value.

5.1 Clock Source Mode

The clock source mode includes the external mode and the internal mode.

- The external clock mode gets clock sources from external circuits such as the EC mode of external clocks, the XT and LP mode of crystal resonators.
- The internal clock mode is built in the oscillator module. The oscillator module has a 16 MHz high frequency oscillator and a 32 kHz low frequency oscillator.

Internal or external clock sources can be selected by the system clock selection bit(SCS) of the OSCCON register.

5.2 External Clock Mode

5.2.1 EC Mode

The external clock mode allows an external logic level as a system clock source. When working in this mode, the external clock source is connected to the OSC1 input.

When the EC mode is selected, the oscillator start-up timer (OST) is disabled. Therefore, there is no delay for operations after the power-on reset (POR) or wake-up from sleep. When the MCU is waken up, the external clock is restarted, and the device is restored to operate as if it has not stopped.

5.2.2 LP and XT Modes

The LP and XT modes support connecting to quartz crystal resonators or ceramic resonators through OSC1 and OSC2 pins. The mode selects the low or high gain settings of the internal inverter-amplifier to support various resonator types and speeds.

The LP oscillator mode selects the lowest gain settings of the internal inverter-amplifier. The LP mode consumes less current than the XT mode. The LP mode is designed only to drive the 32.768 kHz tuning fork based crystals (clock crystal oscillator).

The XT oscillator mode selects the high gain settings of the internal inverter-amplifier.

5.3 Internal Clock Mode

The oscillator mode has 2 independent internal oscillators, which can be configured or selected as the system clock source.

1. The high frequency internal oscillator(HFINTOSC) is calibrated in factory setting with an operating frequency of 16 MHz.
2. The low frequency internal oscillator(LFINTOSC) with an operating frequency of 32 kHz is un-calibrated. It supports system clock speed selection by operating the internal oscillator frequency selection bit IRCF<2:0> of the OSCCON register via software.

The system clock can be selected from external and internal clock sources via the system clock selection bit (SCS) of the OSCCON register.

Notes:

1. The LFMOD of the OSCCON register can select the LFINTOSC as 32 kHz or 256 kHz, however WDT is fixed with 32 kHz, regardless of the LFMOD value.

5.3.1 Frequency Selection Bit (IRCF)

The output of 16 MHz HFINTOSC and 32 kHz LFINTOSC is connected to the prescaler and multiplexer. The OSCCON register's internal oscillator frequency selection bit IRCF<2:0> is used to select the frequency output of the internal oscillator. Select 1 of the following 8 frequencies via the software.

- 16 MHz
- 8 MHz
- 4 MHz (Default value after reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz

- 32 kHz

5.3.2 Clock Switching Timing of HFINTOSC and LFINTOSC

When switching between LFINTOSC and HFINTOSC, the new oscillator may be in shut-down state to save power as shown in Figure 144, Figure 155. In this case, there is a delay between the IRCF bit of the OSCCON register being modified and the frequency selection taking effect. The LTS and HTS bits of the OSCCON register indicate the current state of the LFINTOSC and HFINTOSC oscillators. The frequency selection timing is as follows.

1. The IRCF<2:0> bit of the OSCCON register is modified.
2. If the new clock is shut down, start a clock start-up delay.
3. The clock switching circuit waits for the arrival of the falling edge of the current clock.
4. Keep CLKOUT to low, the clock switching circuit waits for the arrival of 2 falling edges of the new clock.
5. The CLKOUT is connected with the new clock now, and the HTS and LTS bits of the OSCCON register are updated as required.
6. The clock switch completes.

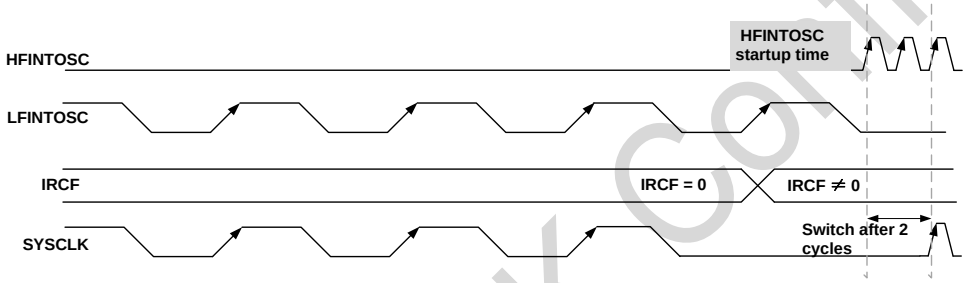


Figure 14. Switch from Slow Clock to Fast Clock

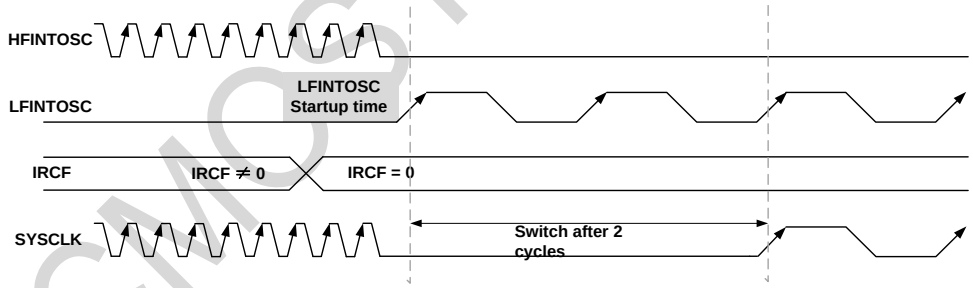


Figure 15. Switch from Fast Clock to Slow Clock

5.4 Clock Switching

Users can switch the system clock source between the external and internal clock sources by operating the system clock selection (SCS) bit of the OSCCON register via software.

5.4.1 System Clock Selection bit (SCS)

The System Clock Selection bit (SCS) of the OSCCON register selects the system clock sources used for the CPU and peripherals.

- When the system clock selection bit (SCS) of the OSCCON register is 0, the system clock source is determined by configuration of the FOSC<2:0> bit in the configuration word register (UCFG0).
- When the system clock selection bit (SCS) of the OSCCON register is 1, the system clock source is selected according to the internal oscillator frequency selected by the IRCF<2:0> bit of the OSCCON register. SCS is always cleared after a reset,.

Notes:

1. Any clock switching caused by hardware (possibly from two-speed start-up or fail-safe clock monitor) will not update the SCS bit of the OSCCON register. Users should monitor the OSTS bit of the OSCCON register to determine the current system clock source.

5.4.2 Oscillator Start-up Timeout State (OSTS) Bit

The oscillator start-up timeout state (OSTS) bit of the OSCCON register is used to indicate whether the system clock is from the external clock source or the internal clock source. The external clock source is defined by the FOSC<2:0> bit in the configuration word register (UCFG0). OSTS also indicates whether the oscillator start-up timer (OST) is timeout in the LP or XT mode.

5.5 Two-Speed Clock Start-up Mode

The two-speed start-up mode reduces the power consumption further by minimizing the latency between the external oscillator and the code execution. For applications using the sleep mode frequently, the two-speed start-up mode removes the external oscillator start-up time after a device wakes up thus reducing the overall power consumption of the device. This mode allows an application to execute several instructions using INTOSC as the clock source then enter sleep again with no need to wait for the startup of the main oscillator.

Notes:

1. Executing a SLEEP instruction will abort the oscillator start-up time and clear the OSTS bit of the OSCCON register.

When the oscillator module is configured as the LP mode or XT mode, the oscillator start-up timer (OST) is enabled. (See Section 5.4.2 for details). OST will suspend the program execution until 1024 oscillations are counted. The two-speed start-up mode minimizes the delay in code execution by operating from the internal oscillator as OST is counting. When OST count reaches 1024 and the OSTS bit of the OSCCON register is set to 1, the program will switch to the external oscillator.

5.5.1 Two-Speed Start-up Mode Configuration

The two-speed start-up mode is configured by the following settings.

- Configure the IESO bit in the Configuration Word register UCFG1 as 1, namely the internal/external switching bit (enable the two-speed start-up mode).
- Configure the SCS bit of the OSCCON register as 0.

- Configure the FOSC<2:0> in the Configuration Word register CONFIG as the LP or XT mode.

It enters the two-speed start-up mode after the steps below.

- Power-on reset (POR) and start power-on timer (PWRT).
- Timer ends (if it is enabled) or wake-up from sleep.

If the external clock oscillator is configured as a mode other than the LP and XT mode, the two-speed start-up will be disabled since the external clock oscillation does not require any stabilization time after POR or exiting from sleep.

5.5.2 Two-Speed Start-up Sequence

1. Wake-up from sleep or power-on reset.
2. Execute instructions using the internal oscillator at the frequency set in the IRCF<2:0> bit of the OSCCON register.
3. The OST instruction counts 1024 clock cycles.
4. The OST is timeout waiting for the falling edge of the internal oscillator.
5. OSTS is set to 1.
6. The system clock keeps low until the next falling edge the new clock arrives (LP or XT mode).
7. The system clock is switched to the external clock source.

5.6 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue operating in the event of an oscillator failure. FSCM can detect the oscillator failure at any time after the oscillator start-up timer (OST) expires. FSCM can be enabled by setting the FCMEN bit in the configuration word register（UCFG1）to 1. FSCM can be used for all external oscillator modes (LP, XT and EC).

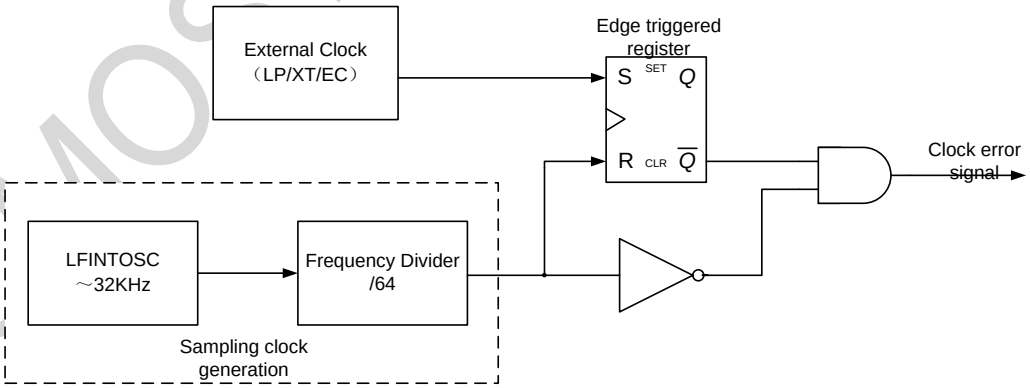


Figure 16. FSCM Schematic

5.6.1 Fail-Safe Detection

The FSCM module detects the oscillator fault by comparing the external oscillator with the FSCM sampling clock. LFINTOSC divided by 64 is the sampling clock. See Figure 16 for details . There is a latch inside the fault detector. On each falling edge of

the external clock, the latch is set to 1. On each rising edge of the sampling clock, the latch is cleared. If the main clock is still not in the low level after a half cycle, it is detected as a fault.

5.6.2 Fail-Safe Operation

When the external clock fault occurs, the FSCM switches the device clock to the internal clock source, and the OSFIF flag bit of the PIR1 register is set to 1. If both the OSFIF flag bit and the OSFIE bit of the PIR1 register are set to 1, an interrupt will be generated. The device firmware will have the related handling to deal with problems caused by the fault clock. The system clock will continue to use the internal clock source until the device firmware restarts the external oscillator successfully and switches back to the external operation. The internal clock source selected by FSCM is determined by the IRCF<2:0> bit of the OSCCON register. It can be configured before the fault occurs.

5.6.3 Fail-Safe Condition Clearing

A fail-safe condition is cleared after a reset, an execution of a Sleep instruction, or a reverse of the SCS bit of the OSCCON register. After the SCS bit of the OSCCON register is modified, the OST will be restarted. When OST runs, the device continues to operate with the INTOSC selected by OSCCON. After OST is timeout, the fail-safe condition is cleared and the device will operate with the external clock source. The fail-safe condition must be cleared first then the OSFIF flag can be cleared.

5.6.4 Reset or Wake-up from Sleep

FSCM is designed to detect oscillator faults at any time after oscillator start-up timer (OST) expires. The OST suits for Wake-up from Sleep or any type of reset. The OST cannot be used in the EC clock mode, so once a reset or wakeup completes, the FSCM is in the active state. When the FSCM is enabled, the Two-Speed Start-up is enabled as well. Therefore, when the OST runs, the device is always in the instruction execution state.

Notes:

1. As the range of oscillator start-up time varies greatly, the Fail-Safe circuit is not active during the oscillation startup period (e.g. after exiting reset or sleep). After an appropriate amount of time, users should check the OSTS bit of the OSCCON register to verify whether the oscillator has successfully started and whether the system clock has been switched successfully.

6 Reset Timing

The CMT2189B supports several types of resets as follows.

1. Power-on reset (POR)
2. WDT reset during normal operating
3. WDT wakeup during sleep
4. MCLR pin reset during normal operating
5. /MCLR pin reset during sleep
6. Brown-out reset/low voltage reset (BOR/LVR)

Some registers are not affected in any reset condition. The states of these registers are unknown upon power-on reset, and is not affected by the reset events. Most of the other registers are restored to their reset states when the following reset events occur.

- Power-on reset (POR)
- WDT reset during normal operating
- WDT reset during Sleep
- /MCLR reset during normal operating
- Brown-out reset (BOR)

WDT (watchdog) sleep wakeup will not result in the same reset due to the WDT (watchdog) timeout during normal operating. Since WDT sleep wakeup itself means that the MCU continues to run rather than resets. The reset actions for clearing or setting the /TO and /PD bits depend on different conditions. See Table 87. Timeout in Various Casesand Table 88 for details.

The circuit corresponding to the /MCLRB pin supports the anti shake function. It can filter the sharp pulse signal caused by interference. See the overall block diagram of the reset circuit in the below figure.

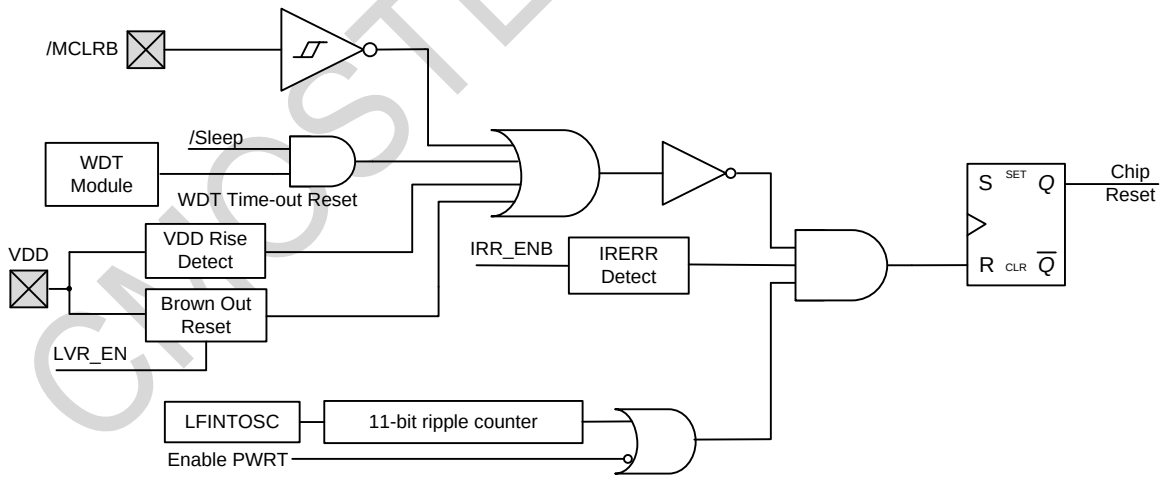


Figure 17. Reset Function Block Diagram

6.1 Power-on Reset (POR)

The on-chip POR circuit will keep the chip in the reset state until VDD reaches a high enough level. To use the on-chip POR function, users can simply set a resistor between the /MCLR and the VDD with no need for an external RC Reset circuit. However it requires the VDD rising time remains the maximum. When power-on completes, the system reset will not be released immediately. There is a delay time for about 4 ms, during which the digital circuit keeps in the reset state.

6.2 MCLR External Reset (MCLR)

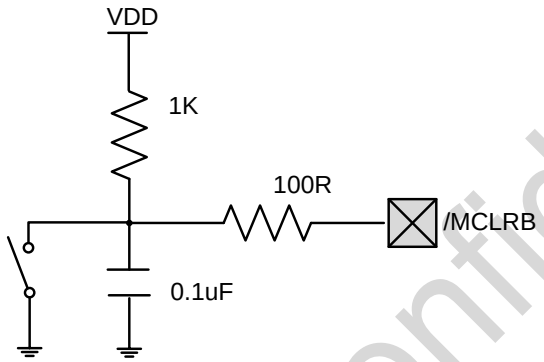


Figure 18. External Reset Reference Circuit Diagram

The chip's CONFIG OPTION register (UCFG0) has a MCLRE enabling bit. When this bit is 0, the reset signal is generated inside the chip. When this bit is 1, the PA5/MCLR pin of the chip becomes the external reset pin. In this mode, the /MCLR pin has a weak pull-up for VDD.

6.3 Power-up Timer (PWRT)

PWRT provides a fixed 64 ms timing (in normal case) for power-on reset and brown-out reset. This timer is driven by an internal slow clock. The chip keeps in the reset state before the timeout of the timer. This time ensures that VDD will rise to a sufficiently high voltage to make the system operate properly. PWRT can also be enabled by the system CONFIG register (UCFG0). When the low voltage reset function is enabled, users should also enable PWRT. The PWRT timing is triggered by a VDD voltage exceeding the VBOR threshold. It is also important to know that the actual time changes with temperature and voltage as it is driven by the internal slow clock drive, thus this time is not a precise parameter.

6.4 Brown-out Reset / Low Voltage Reset

The low voltage reset refers to the reset occurring when the power supply voltage is lower than the VBOR threshold voltage, which is controlled by UCFG1<1:0> bit. However, the low voltage reset may not occur when the VDD voltage is lower than VBOR and the time does not exceed TBOR. The VBOR voltage needs to be calibrated before the chip shipping. The calibration can be fulfilled by writing the internal calibration register through the serial port. If the BOR (brown-out reset) is enabled (UCFG1<1:0>=00), it does not have the requirement on the maximum VDD voltage rising time. The BOR circuit will control the chip in the reset state until the VDD voltage exceeds the VBOR threshold voltage. It is important to know that the POR circuit does not generate a reset signal when the VDD is lower than the threshold on which the system can operate normally. If the reset signal is generated by the BOR circuit, the VDD voltage must keep for more than 100 us at the VSS level.

6.5 Error Instruction Reset

When the instruction register of the CPU obtains an undefined instruction, the system will have reset, which help improve the system anti-interference ability.

6.6 Timeout Action

During the power-on process, the internal timeout action sequence of the chip is as follows. The PWRT timing is started after the POR ends. As the timing is started by the POR pulse, a timeout will occur if the /MCLR keeps low for a long enough time. Pulling the /MCLR high will make the CPU to start the executing immediately, which is useful for testing or implementing multiple MCU synchronization.

PCON（Power Control Register）

There are 2 state bits in the PCON register to indicate what type of reset occurs. Bit 0 is the /BOR bit, of which the state is unknown upon power-on reset, thus the software must set it to 1 and check whether it is 0 then. Bit 1 is the /POR indication bit, which is 0 upon power-on reset, and the software must set it to 1.

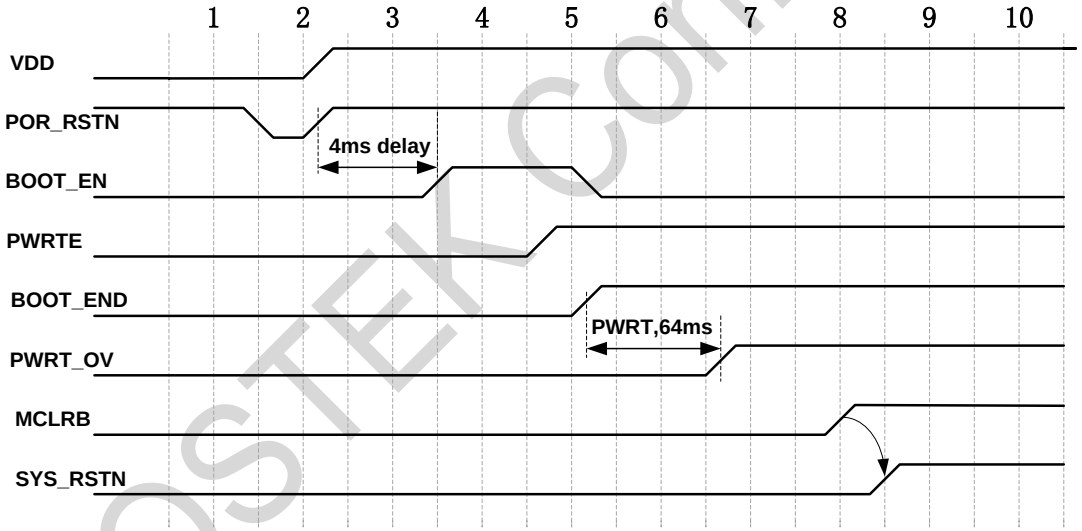


Figure 19. Power-on Reset with MCLRB

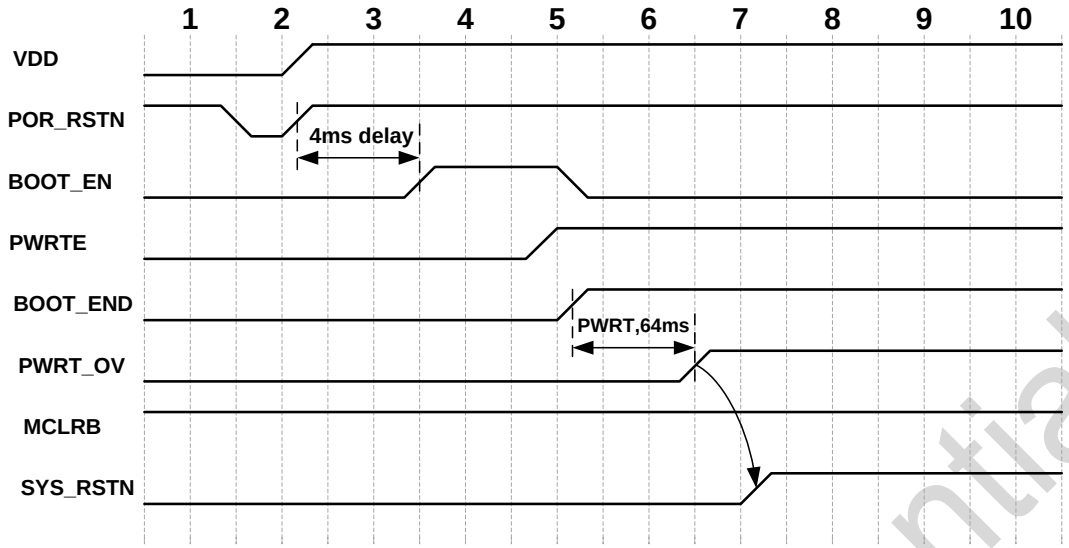


Figure 20. Power-on Reset without MCLRB

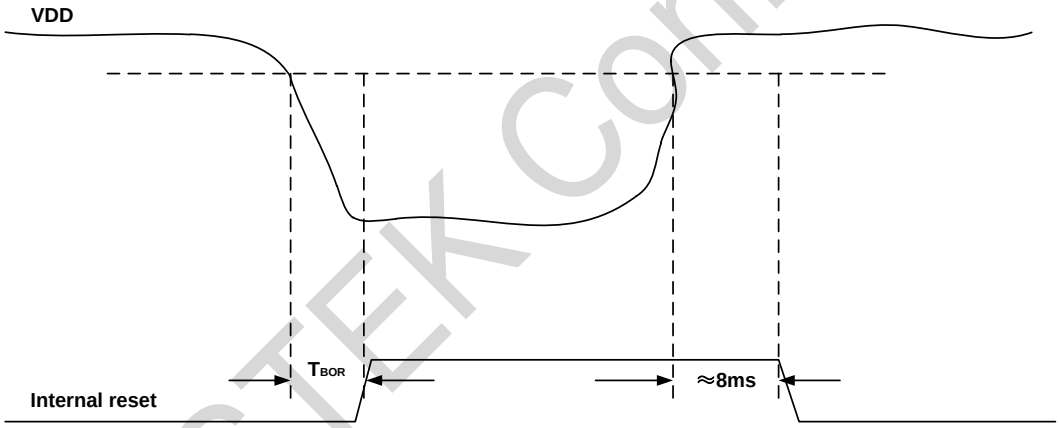


Figure 21. BOR Reset

Notes:

1. After POR or BOR, if PWRTEB (UCFG0.4) is low, PWRT is active, which keeps 2048 internal slow clock cycles, about 64 ms.
2. The TBOR time is about 157 us.
3. After the voltage is restored to normal, the internal reset will not be released immediately, but wait for about 8 ms instead.

Table 87. Timeout in Various Cases

Oscillator configuration	Power-on Reset		Brown-out Reset		Sleep Wake-up
	/PWRTEB=0	/PWRTEB=1	/PWRTEB=0	/PWRTEB=1	
INTOSC	TPWRT	-	TPWRT	-	-

Table 88. STATUS/PCON Bit Description (U: no change, X: unknown)

/POR	/BOR	/TO	/PD	Condition
0	X	1	1	POR
U	0	1	1	BOR
U	U	0	U	WDT Reset
U	U	0	0	WDT Wake-up
U	U	U	U	/MCLR reset during normal operation
U	U	1	0	/MCLR reset during sleep

7 BOOT

After POR or BOR, it inserts a state and maps the program EEPROM units starting from 2000H into configuration registers. The system reset is released until the end of the BOOT, as shown in Figure 19 and Figure 20. The process needs about 17 us.

8 Watchdog Timer

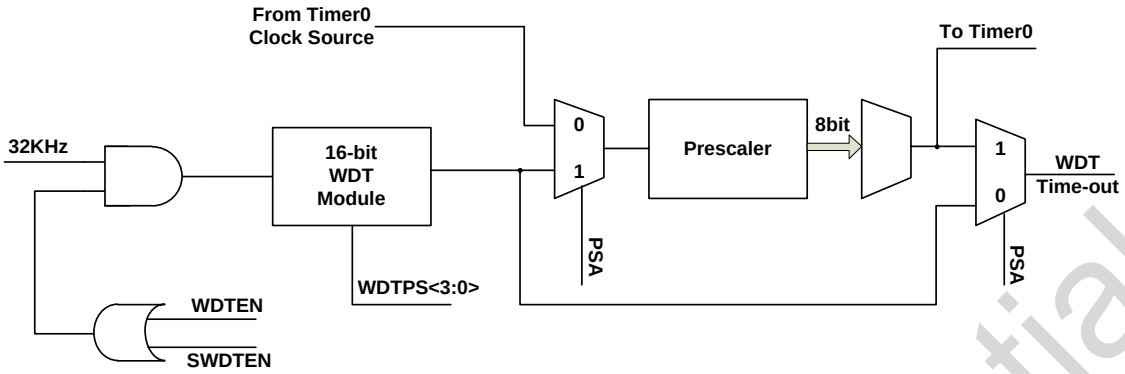


Figure 22. Watchdog and Timer 0 Diagram

The watchdog's clock source is the internal slow clock (32 kHz), which is a 16-bit counter. It shares an 8-bit prescaler with Timer 0. The enabled bit WDTEN is the 3rd bit of the configuration register UCFG0. When the WDTEN is 1, it enables the watchdog. When it is 0, disable. It is determined by BOOT during the power-on process, or it can be written through the external serial port. The CLRWDT instruction for clearing the watchdog and SLEEP instruction will clear the watchdog counter. In the case of enabling the watchdog, the watchdog overflowing can be used as a wake-up source when the MCU is in the sleep state, and the watchdog can be used as a reset source when the MCU operates in normal status.

Table 89. Watchdog Status

Condition	Watchdog Status
WDTEN and SWDTEN are 0 at the same time	Cleared
CLRWDT instruction	
Enter the SLEEP, exit the SLEEP	

Notes:

1. If the internal slow clock switches from the 32 k to 256 k mode (or from the 256 k to 32 k mode), it does not affect the watchdog timing, as WDT is fixed to use the 32 k clock source.

9 Timer 0

9.1 Timer0 Introduction

The timer can be configured as a 8-bit counter or timer. When it is used as the external event (T0CKI) counter, it can count on the rising edge or the falling edge. When it is used as a timer, the counting clock is the system clock divided by 4, namely, it increases once in each instruction cycle. It has an 8-bit prescaler shared with the WDT. When the PSA bit is 0, the prescaler is assigned to Timer 0.

Notes:

1. When the value of PSA is changed, the hardware will clear the prescaler automatically.

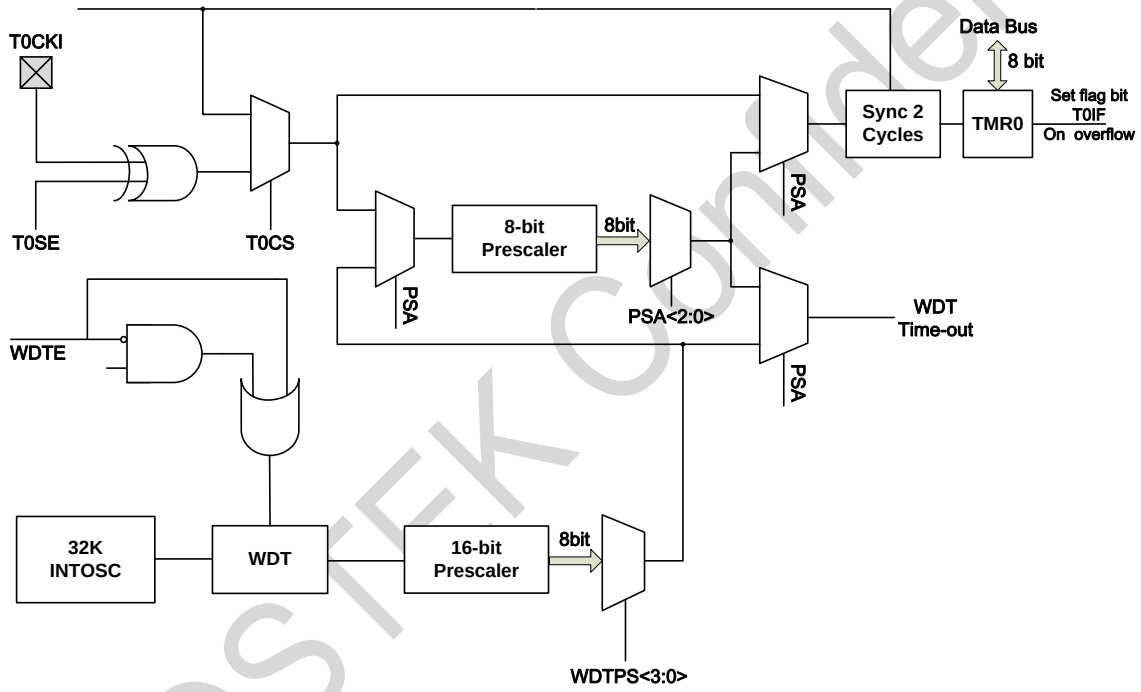


Figure 23. Watchdog and Timer 0 Diagram

9.2 Timer Mode of Timer 0

In this mode, Timer 0 increases by 1 (without prescaler) in each instruction cycle. The software can clear the T0CS bit of the OPTION register to enter the timer mode. When the software performs write operation to the TMR0, the timer will not increase in the following 2 cycles.

9.3 Counter Mode of Timer 0

In this mode, the timer 0 increases by 1 when it is triggered by each rising or falling edge of the T0CKI pin (without prescaler). Which edge to trigger is determined by the T0SE bit of the OPTION register. The software can set the T0CS bit of OPTION register to 1 to enter the counter mode.

9.3.1 Prescaler Circuit Configurable by Software

The chip has a prescaler circuit in front of the Timer 0 and WDT timer, which can be assigned to Timer 0 or the WDT timer, but they cannot use the prescaler at the same time. Whether assign to Timer0 or WDT is determined by the PSA bit of the OPTION register. When PSA is 0, the prescaler is assigned to Timer 0. In the Timer 0 prescaler mode, there are 8 prescale ratios (1:2 to 1:256), which can be set by the PS<2:0> bit of the OPTION register.

Notes:

1. The prescaler circuit is neither readable nor writable. Any write operation on the TMR0 register will clear the prescaler circuit.
2. When the prescaler circuit is assigned to the WDT, the prescaler circuit can be cleared by 1 CLRWDT instruction.
3. The prescaler circuit can be assigned to Timer 0 or the WDT timer, the prescaler switching between Timer 0 and WDT may result in a false reset.

When switch the prescaler assignment from TMR0 to WDT, please execute the following instruction sequence.

```
BANKSEL   TMR0
CLRWDT                          ; Clear WDT
CLRR      TMR0                  ; Clear TMR0 and prescaler
BANKSEL   OPTION_REG
BSR       OPTION_REG,  PSA      ; Select WDT
CLRWDT


LDWI      b'11111000'           ; Mask prescaler bits
```

When switch the prescaler assignment from the WDT to TMR0, please execute the following instruction sequence.

```
CLRWDT                          ; Clear WDT and prescaler
BANKSEL   OPTION_REG
LDWI      b'11110000'           ; Mask TMR0 select and prescaler bits
ANDWR     OPTION_REG, W
```

9.3.2 Timer 0 Interrupt

An interrupt is generated (if the interrupt is enabled) when the TMR0 timer overflows from 0xFF to 0x00. This overflow sets the T0IF bit.

Notes:

1. Timer 0 interrupt cannot wake up the CPU from the sleep state since the timer is switched off during sleep.

9.3.3 Timer 0 Driven by External Clock

In the counter mode, the synchronization between the T0CKI pin input and the Timer 0 register is fulfilled by sampling the phase of the internal clock Q1 and Q2, therefore the high level time and low level time of the external clock source cycle must meet the relevant timing requirement.

10 Timer 2

The timer2 is an 8-bit timer, which supports the following functions:

- 8-bit count register
- 8-bit period register
- Interrupt on TMR2 matching with PR2
- Frequency prescaler ratio of 1:1, 1:4 and 1:16
- Postscaler ratio ranging from 1:1 to 1:16

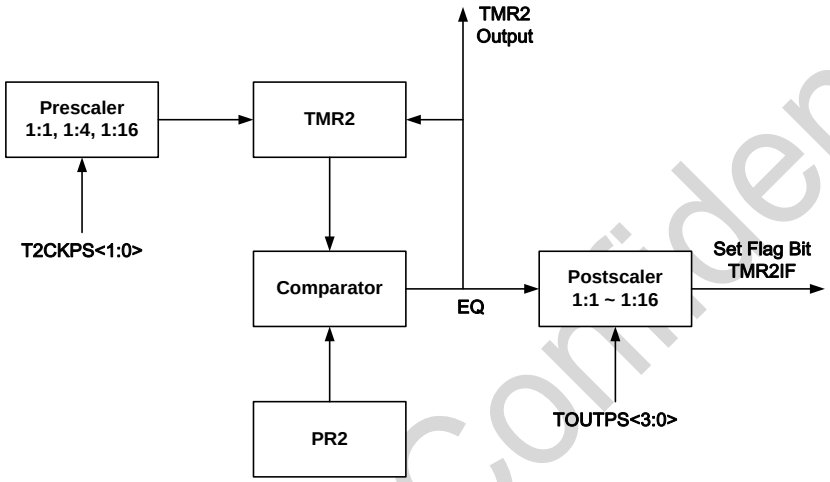


Figure 24. Timer2 Block Diagram

Timer 2 operating principle

The system instruction clock (FOSC/2) is the clock input of the Timer2 module, which is sent to the Timer 2 prescaler with 3 prescale ratio options, 1:1, 1:4 and 1:16. Then the output of the prescaler is used to increase the TMR2 register.

The values of TMR2 and PR2 are compared constantly to determine when to match. The TMR2 will increase from 00h until it matches the PR2. The followings will occur when they match.

- TMR2 is reset to 0x00 in the next cycle for increasing
- The Timer 2 postscaler ratio increases progressively.

The matching output of comparing Timer2 and PR2 is sent to the postscaler of Timer 2 with a division ratio ranging from 1:1 to 1:16. The output of the postscaler of Time r2 is used to set the interrupt flag bit TMR2IF of the PIR1 register to 1.

Note:

1. Both TMR2 and PR2 are read-write registers. Their values are initialized to 0 and 0xFF respectively upon reset.
2. Setting the TMR2ON bit of the T2CON register to 1 can enable Timer 2, and clearing the TMR2ON bit can disable Timer 2 on the contrary.
3. The Timer 2 prescaler is controlled by the T2CKPS bit of the T2CON register.
4. The Timer 2 postscaler is controlled by the TOUTPS bit of the T2CON register.

5. The prescaler counter and postscaler counter will be cleared when the following registers are written:

- Write the TMR2
- Write the T2CON
- Any reset action

6. Writing the T2CON does not clear the TMR2 register.

11 Comparator

2 analog comparators are integrated in the chip. As the function pins of the comparator 2 are used for the RF serial control bus at the same time, the 2 comparators cannot be used.

It should be noted that, when reading a port register, the software reading value is 0 if the pin is configured as an analog signal pin. Even when the pin is set as a digital input pin, the comparator will still regard the pin will input an analog signal thus output the corresponding result. If the pin is set as a digital input, however the actual voltage on this pin is still an analog voltage, it may cause the input buffer circuit to consume more current than that in the specifications.

The analog comparator supports 8 configuration modes. They are selected by the CM<2:0> bit of the CMCON0 register. However, only 2 states are supported as shown in the below figure, since the functional pins are used in the RF serial control bus.

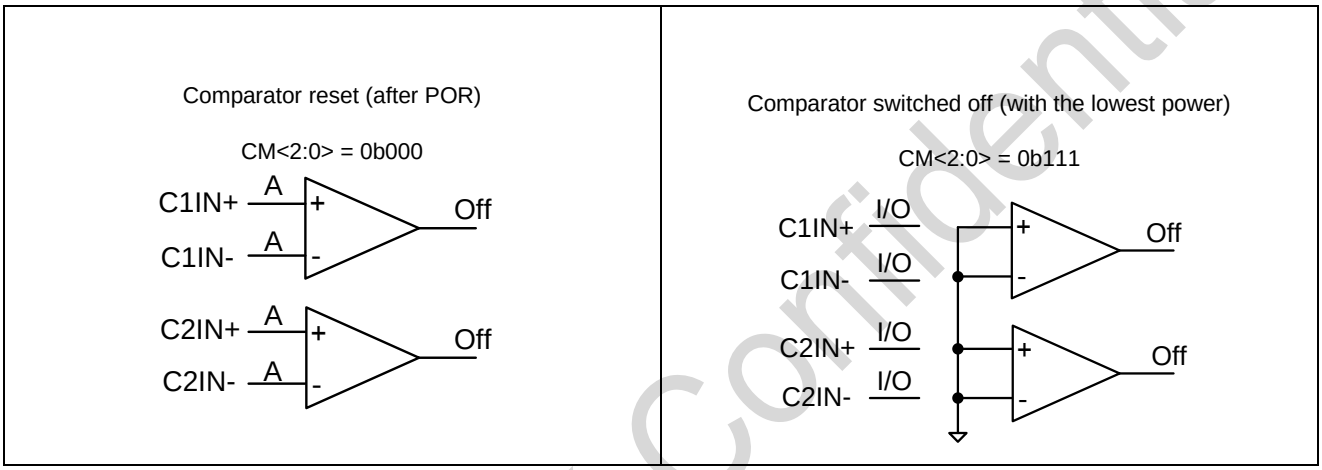


Figure 25. 2 Configuration Modes of Analog Comparator

- Analog function (A): the digital input buffer is disabled.
- Digital function (D): the comparator digital output will override the other functions in the pin
- Normal port function (I/O): it is independent of the comparator.

When the word A is marked on the port, the current pin states of the TRIS bit of the I/O control register will return to 0 per read operation. The TRIS bit, a bit corresponding to the analog input pin, should be set to1 to close its digital output drive circuit.

When the word D is marked on the port, users should set the corresponding TRIS bit to 0 to open the digital output driver circuit.

In addition, the comparator interrupt should be disabled during the comparator configuration switching to avoid unexpected miss-triggered events.

12 Data EEPROM

The chip is integrated with a 256-byte EEPROM, which is accessed through the EEADR. It supports the software programming the EEPROM through the EECON1 and EECON2. The erasing and programming function is implemented by the hardware with no need for software query, which saves the limited code space. Meanwhile, by using this feature, it supports the chip enters the sleep mode after starting the programming cycle to reduce power consumption.

The following initialization process must be performed before the data EEPROM is used (either read or write), that is, write double 0xAA to an unused EEPROM unit, and make sure the program will no longer operate this unit after then. The code example is as follows.

```
SYSTEM_INIT
......
......
LDWI    0x55
STR     EEROM_ADDR
LDWI    0xAA
STR     EEPROM_DATA
LCALL   EEPROM_WRITE
LCALL   EEPROM_WRITE
```

Steps for data EEPROM programming

To read a data memory unit, users must write the address into the EEADR register, and then set the control bit RD of the EECON1 register to 1. In the next cycle, the EEDAT register is written with the EEPROM data. Therefore, this data can be read by the next instruction. The EEDAT will keep this value until the user reads or writes the data of the unit the next time (during the write operation).

```
BANKSEL   EEADR
LDWI      dest_addr
STR       EEADR
BSR       EECON1,RD
```

13 Clock Measurement

This function can measure the internal slow clock period accurately.

In this mode, the prescaler and postscaler configuration of TIMER2 is automatically changed to 1:1, which forms a 12-bit timer. The TIMER2 count clock is the system clock Fosc, but not the instruction clock Fosc/2 as in ordinary modes. After the count ends, the result is automatically stored in the SOSCPR register with the unit as the number of the system clock2 Fosc.

The operation steps are as follows.

1. To improve the measurement accuracy, it is suggested that IRCF is set to 111 and SCS is set to 1, and the system clock of 16 M is selected.
2. Set T2CON.2 to 1 and enable TIMER2.
3. If selecting the average of four measurement values, set MSCKCON.2 to 1, otherwise clear it.
4. Set MSCKCON.1 to start measuring.
5. After the end of the measurement, MSCKCON.1 is automatically cleared, and the interrupt flag is set to 1.
6. Wait for the measurement completion in a query or interrupt manner.
7. When the interrupt flag is checked to be 1, the read SOSCPR is the final result.

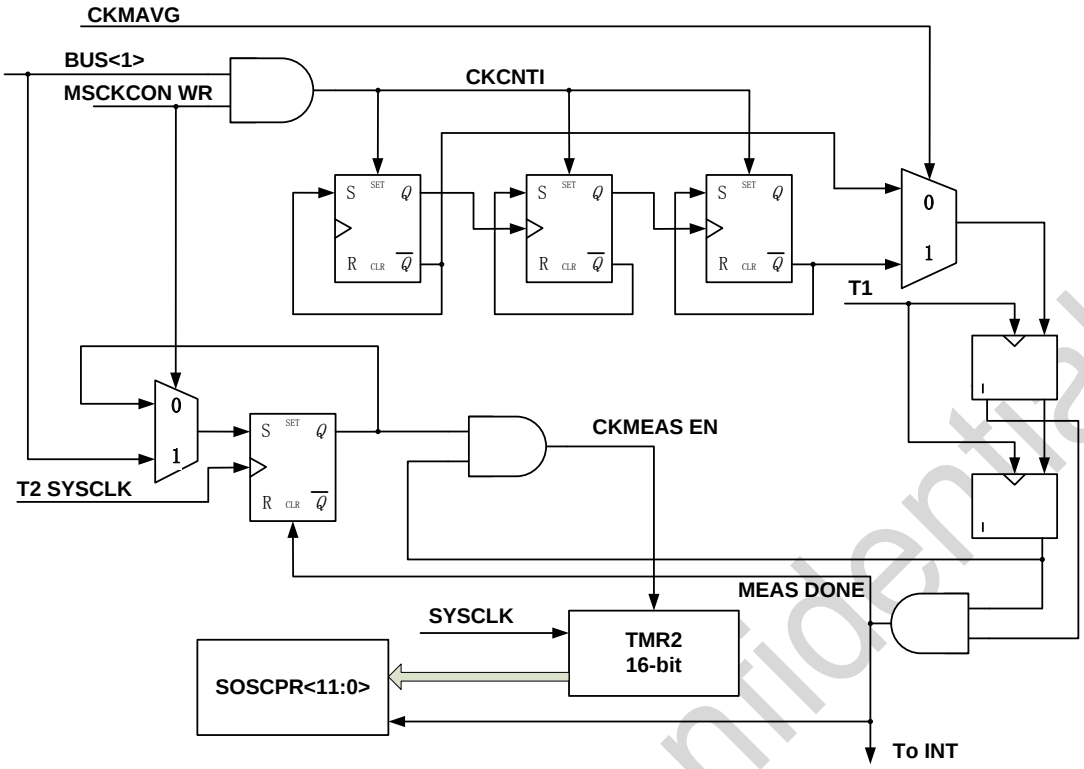


Figure 26. Block Diagram for Slow Clock Measurement Mode

14 Interrupt Mode

The CMT2189B supports the following interrupt sources:

- External interrupt from the PA2/INT pin
- Timer 0 overflow interrupt
- PORTA change Interrupt
- Timer 2 compare matching interrupt
- EEPROM data write Interrupt
- Slow clock measurement Interrupt

The interrupt control register (INTCON) and peripheral interrupt request register (PIR1) record the interrupt flag bit. The INTCON also contains the global interrupt enabling (GIE) bit.

When an interrupt is served, the following actions are performed automatically.

- GIE is cleared to close the interrupt.
- The return address is pushed onto the stack.
- The program pointer is loaded with the 0004h address.

The return from Interrupt instruction (RETFIE) exits the interrupt routine, as well as sets the GIE bit, which re-enable the unblocked interrupts.

The INTCON register contains the following interrupt flag bits.

- INT pin interrupt
- PORTA change interrupt
- Timer 0 overflow interrupt

PIR1 contains the peripheral interrupt flag bit and PIE1 contains its corresponding interrupt enabling bit.

14.1 INT Interrupt

The external interrupt of the INT pin is triggered by edges. When the INTEDG bit of the OPTION register is set to 1, it is triggered on the rising edge. It is triggered on the falling edge when the INTEDG bit is cleared,. When an effective edge occurs on the INT pin, the INTF bit of the INTCON register is set to 1. The interrupt can be disabled by clearing the INTE control bit of the INTCON register. Before the interrupt is re-enabled, the INTF bit must be cleared by the software in the interrupt service routine. If the INTE bit is set to 1 before entering the sleep state, the INT interrupt can wake up the MCU from the sleep state.

Notes:

1. When using the INT interrupt, users should initialize the ANSEL and CM2CON0 registers so that the analog channel is configured as a digital input. The pin configured as an analog input is always read as 0.

14.2 PORTA Level Change Interrupt

The input change on the PORTA will set the PAIF bit of the INTCON register. The interrupt can be enabled or disabled by setting/clearing the PAIE bit. In addition, each pin of the port can be configured through the IOCA register.

Notes:

1. When using the PORTA level change interrupt, users should initialize the ANSEL and CM2CON0 registers so that the analog channel can be configured as a digital input. The pin configured as an analog input is always read as 0.
2. When initializing the level change interrupt, configure it as a digital input IO first and set the corresponding IOCA to 1, then read the PORTA.
3. When the IO level changes, the PAIF bit is set to 1.
4. Read the PORTA before clear the interrupt flag, then clear PAIF.

14.3 Interrupt Response

The interrupt delay of the external interrupts, including the interrupt from the INT pin or the PORTA change interrupt, is usually 1 to 2 instruction cycles depending on actual interrupt situations.

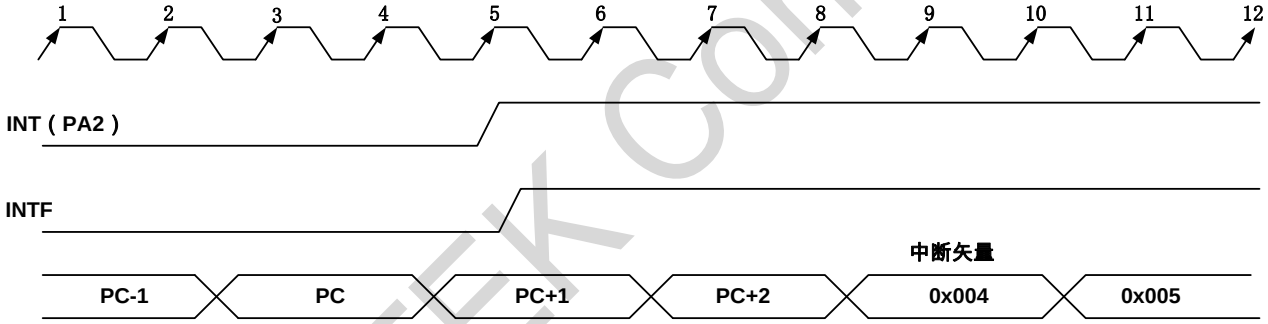


Figure 27. Interrupt Response Timing Diagram

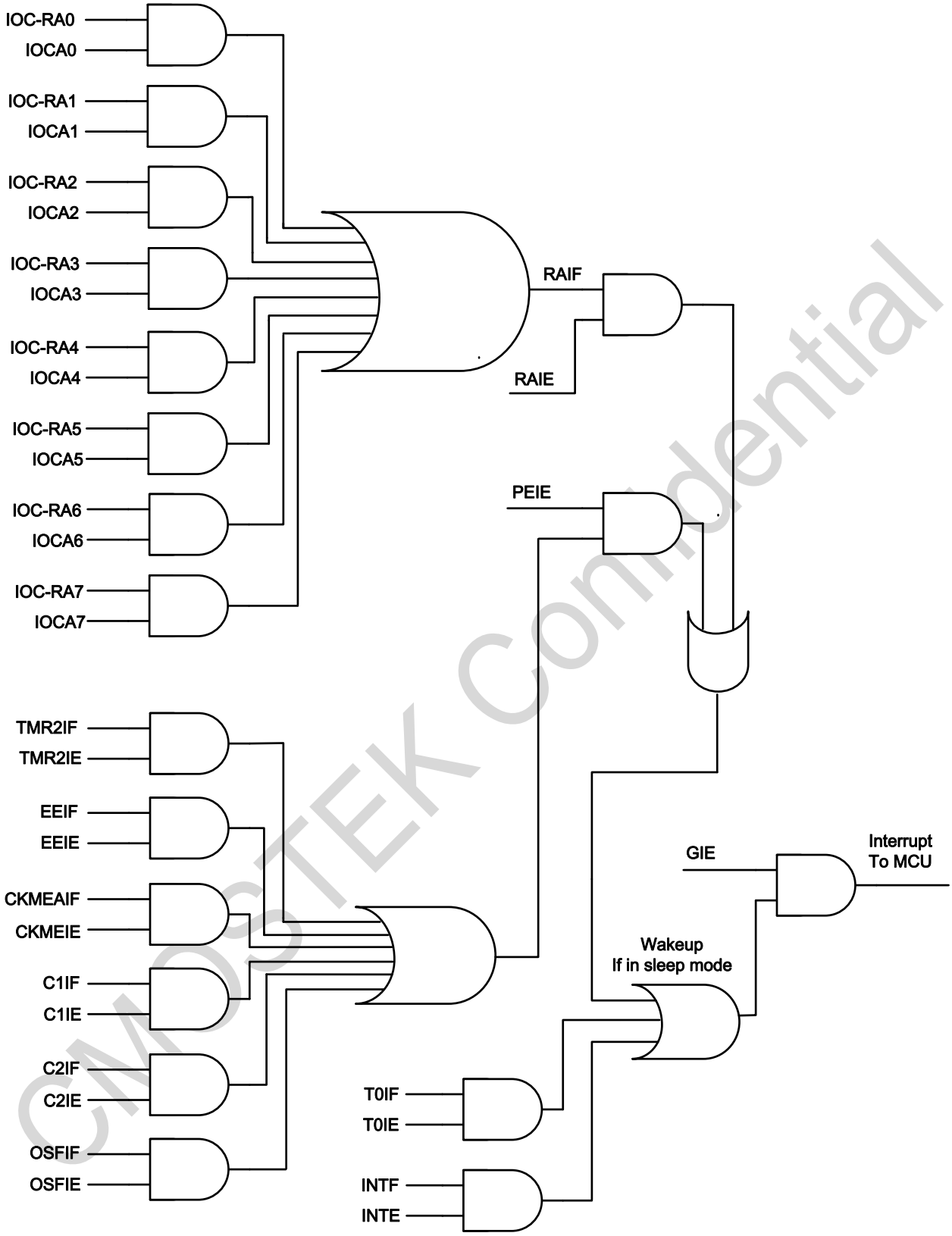


Figure 28. Interrupt Generation Circuit Block Diagram

14.4 Context Saving During Interrupts

During an interrupt, only the return PC is automatically saved on the stack. In general, users may require to save key register values on the stack, such as W, STATUS register, which can be implemented in the software only. The temporary registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR. The 16 bytes of GPR cross two pages, so users can save a little bit of code space.

15 MCU Sleep Mode for Energy Saving

The chip enters the sleep state after the SLEEP instruction execution.

To achieve the lowest sleep power consumption, the software should set all IO to high or low, and ensure no external circuits have power consumption from IO pins. For an input I/O, the external circuit should pull it high or low to avoid power consumption caused by level reverse. The /MCLR should be in high level.

To achieve the lowest power consumption, it is recommended that, users switch off the function when the crystal mode or external clock mode is configured, namely clear the FCMEN bit of the UCFG1. Meanwhile, the configuration bit CM<2:0> of the comparator is written as 0b111 to switch off the comparator module.

15.1 Wakeup Mode

The following events can wake up the chip.

- The external reset on the /MCLR pin.
- WDT timeout.
- Interrupt on the PA2/INT pin, PORTA change interrupt or other peripheral interrupts.

Clearing watchdog (CLRWDT), entering the sleep mode (SLEEP) or waking up from the sleep mode will clear the watchdog counter.

15.2 Watchdog Wake-up

The watchdog operates with the internal slow clock (32 kHz). It is a 16-bit counter, and shares a 8-bit prescaler with Timer 0. The corresponding enabling bit is the 3rd bit WDTEN of the configuration register UCFG0. Set it to 1 to enable the watchdog. When set to 0, whether or not to enable the watchdog depends on the SWDTEN bit. SWDTEN is in the WDTCON register.

Clearing watchdog (CLRWDT) and SLEEP instruction will clear the watchdog counter.

When enabled, the watchdog overflowing event can be used as a wake-up source when the MCU is in sleep mode, while it can be used as a reset source when the MCU operates normally.

16 I/O Port

There are 16 GPIO ports in the chip. However, limited by the package size, only 6 IO ports of PORTA<7:0> have pins (except PA6 and PA5) and PC4 as well as PC6 of PORTC have pins. The others are all inside the chip without pins. In addition to operating as ordinary input / output port, these IO ports generally have functions to communicate with the peripheral circuits of the core. See below for details.

16.1 PORTA Port and TRISA Register

PORTA is an 8-bit bi-directional port with TRISA as its corresponding input/output direction register. However, it should be noted that the 5th bit is not in use here because PORTA<5> is a single directional input port. Setting a certain bit in the TRISA register to 1 will set the corresponding PORTA port as input port (the output driver circuit will be disabled accordingly). On the contrary, setting a certain bit to 0 will set the corresponding PORTA port as output port. When configured as output port, the output driver circuit is enabled and the data in the output register will be sent to the output port. Upon reading the PORTA, the PORTA content will reflect the input port state. Upon writing the PORTA, the PORTA content will be written to the output register. All operations follow the read-modify-write process, namely the data is read first, then modified, and written to the output register after then. When MCLRE is 1, the value read from PORTA<5> is 0, which is used as the external reset pin at this time.

16.2 Other Functions of the Port

A state change interrupt option and a weak pull-up option are available for each port of PORTA.

16.2.1 Weak Pull-Up

Each port of PORTA (except for PORTA<5>) has an internal weak pull-up function that can be set individually. Controlling the bit of the WPUAx register can enable or disable the weak pull-up circuit. When a GPIO is set as output, the weak pull-up circuit is disabled automatically. The weak pull-up circuit can be disabled during the power-on reset period. This is determined by the /PAPU bit of the OPTION register. The weak pull-up function is available as well inside PORTA<5>. The weak pull-up function will be automatically enabled when PORTA<5> is set as /MCLR. When PORTA<5> is set as GPIO, the weak pull-up circuit will be disabled automatically.

16.2.2 Sate Change Interrupt

Each port of the PORTA can be set as an interrupt source (for state change interrupt) separately. Controlling the bit of the IOCAx register can enable or disable the interrupts of these ports. The state change interrupt is invalid upon the power-on reset.

When enabling the state change interrupt, the current port level value is compared to the old value of the data register read by the last reading action. It will perform OR operation on all mismatching results to form an interrupt flag bit. The PAIF flag bit of the INTCON register can wake up the chip from the sleep state. Users need to execute the following program to clear the flag bit.

1. Perform a read or write operation to the PORTA to end any mismatched status.
2. Clear the PAIF flag bit.

The mismatching result will always set the PAIF bit. Reading PORTA once can end any mismatching status to clear the PAIF bit. The last read value kept in the data register will not be affected by /MCLR or BOR. As long as the mismatching status exists, PAIF bit will set to 1.

16.3 Port Description

Each port of PORTA and PORTC contains different multiplexing functions. The specific functions and controls will be discussed in this section.

16.3.1 PORTA<2:0>

PA<2:0> can be configured as the following functional port.

- GPIO
- serial port clock for debug (PA0)
- Serial port data for Debug (PA1)
- External interrupt input (PA2)
- External clock source for Timer0 (PA2)

The following figure describes The internal circuit architecture of the port is shown in the below figure.

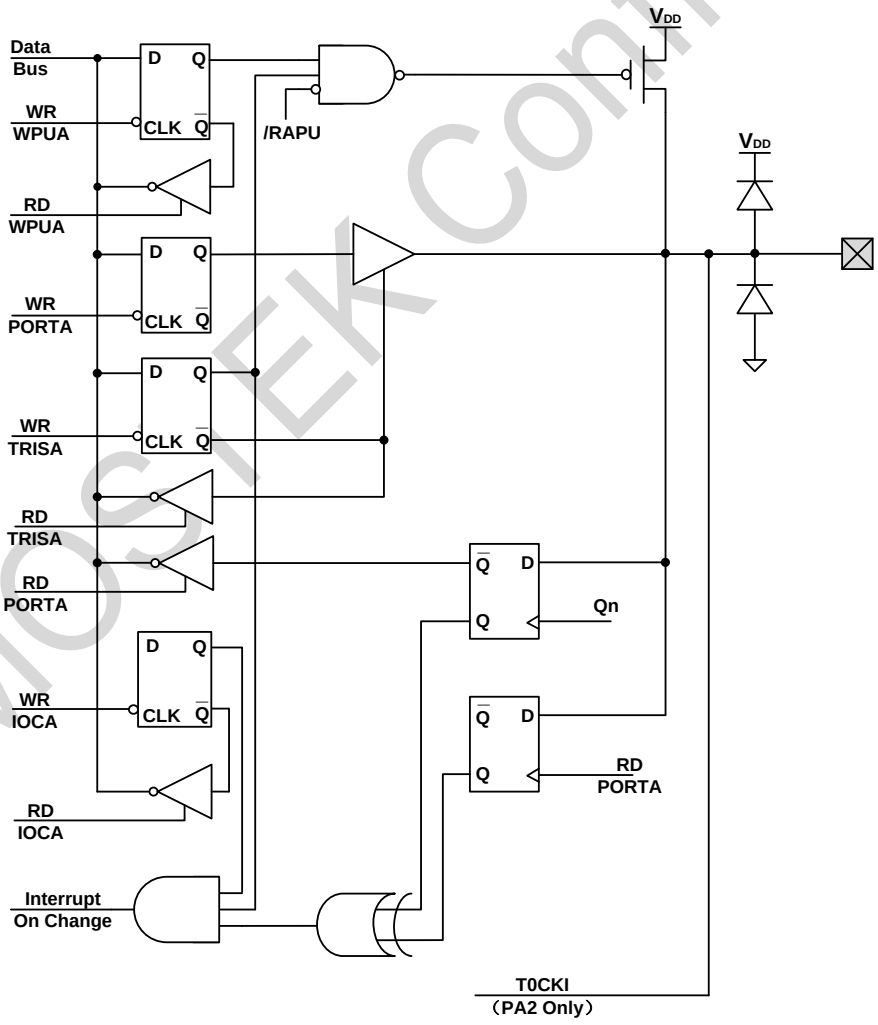


Figure 29. PA<2:0> Architecture Diagram

16.3.2 PORTA3/PA3

PA3 can be configured as the following functional port:

- GPIO

The internal circuit architecture of the port is shown in the below figure.

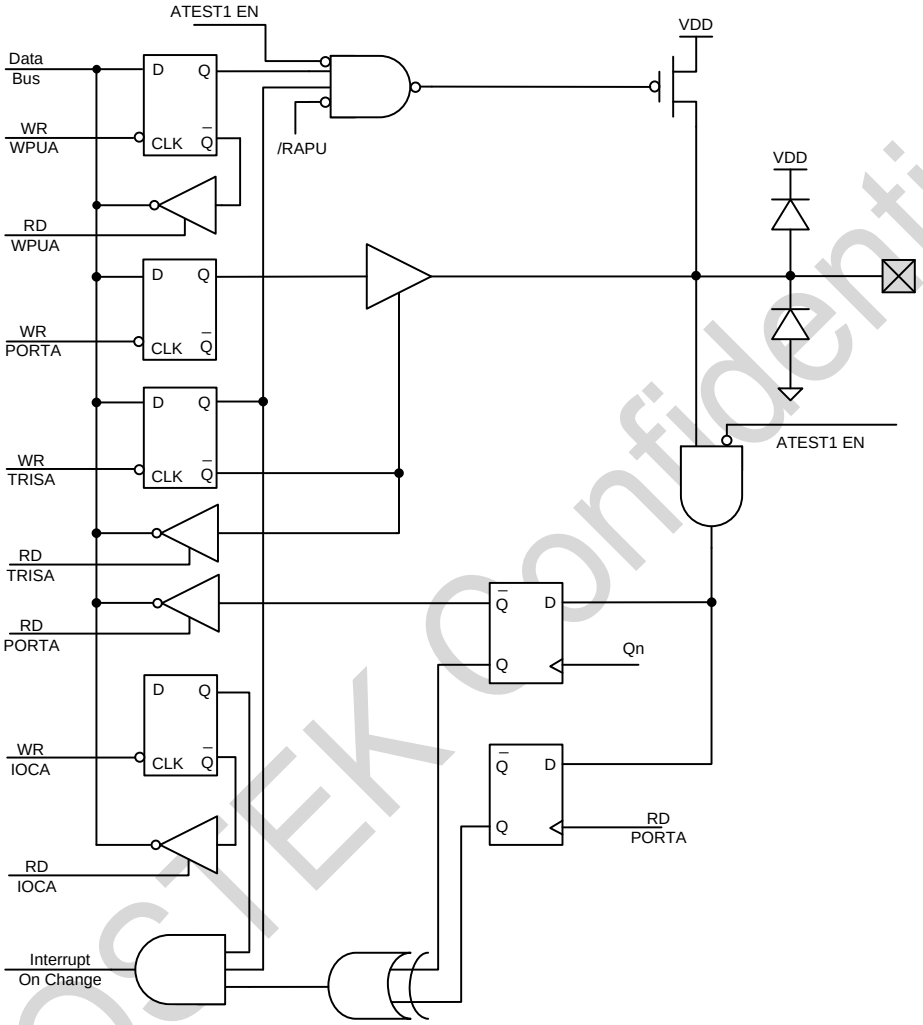


Figure 30. PA3 Architecture

Notes:

1. ATEST1 is used for internal test, but not for users. Users can ignore it.

16.3.3 PORTA4/PA4

PA4 can be configured as the following functional port:

- GPIO

The internal circuit architecture of the port is shown in the below figure.

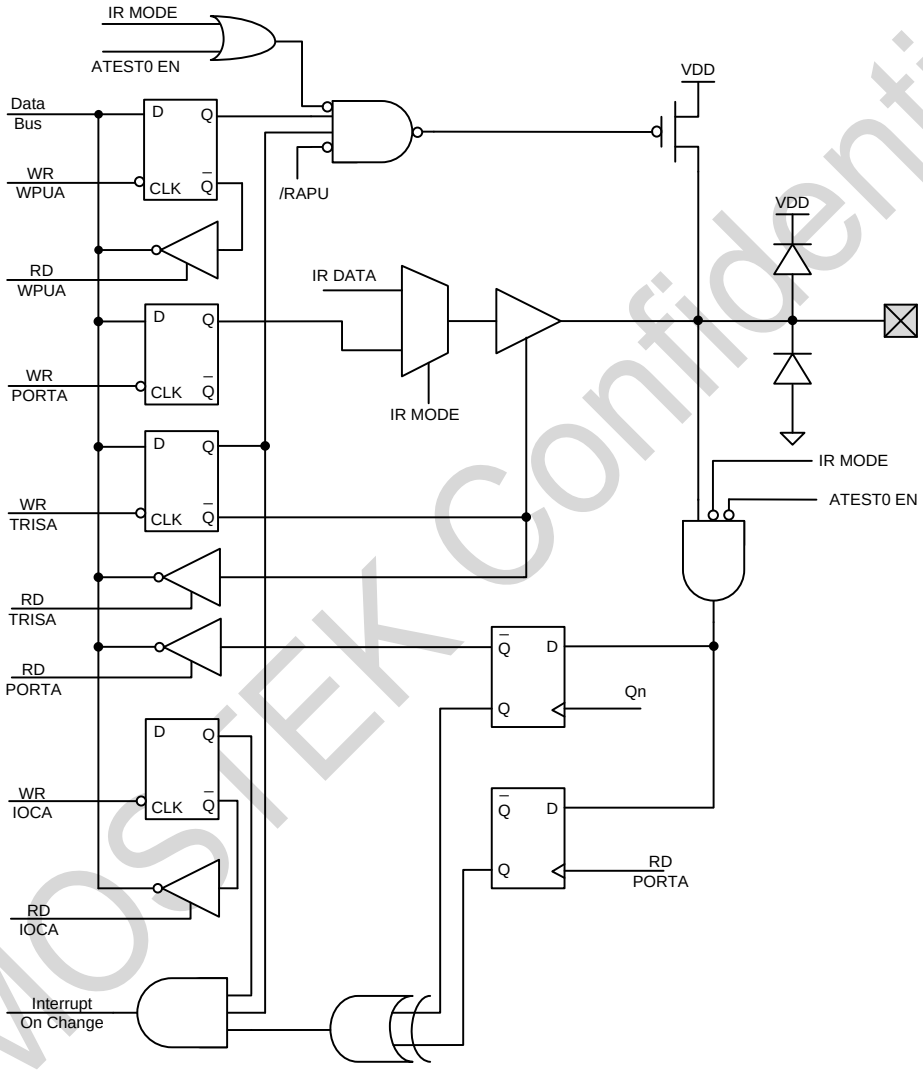


Figure 31. PA4 Architecture

Notes:

1. ATEST0 and IR are used for internal test, but not for users. Users can ignore them.

16.3.4 PORTA5/PA5

Due to package pin limitation, PA5 has no package pin, therefore users can only configure it as an internal reset through the UCFG configuration, and it is not recommended to configure it as an external reset.

16.3.5 PORTA7/PA7

PA7 can be configured as the following functional port:

- GPIO
- Crystal oscillator and resonator connection
- Clock input

The internal circuit architecture of the port is shown in the below figure.

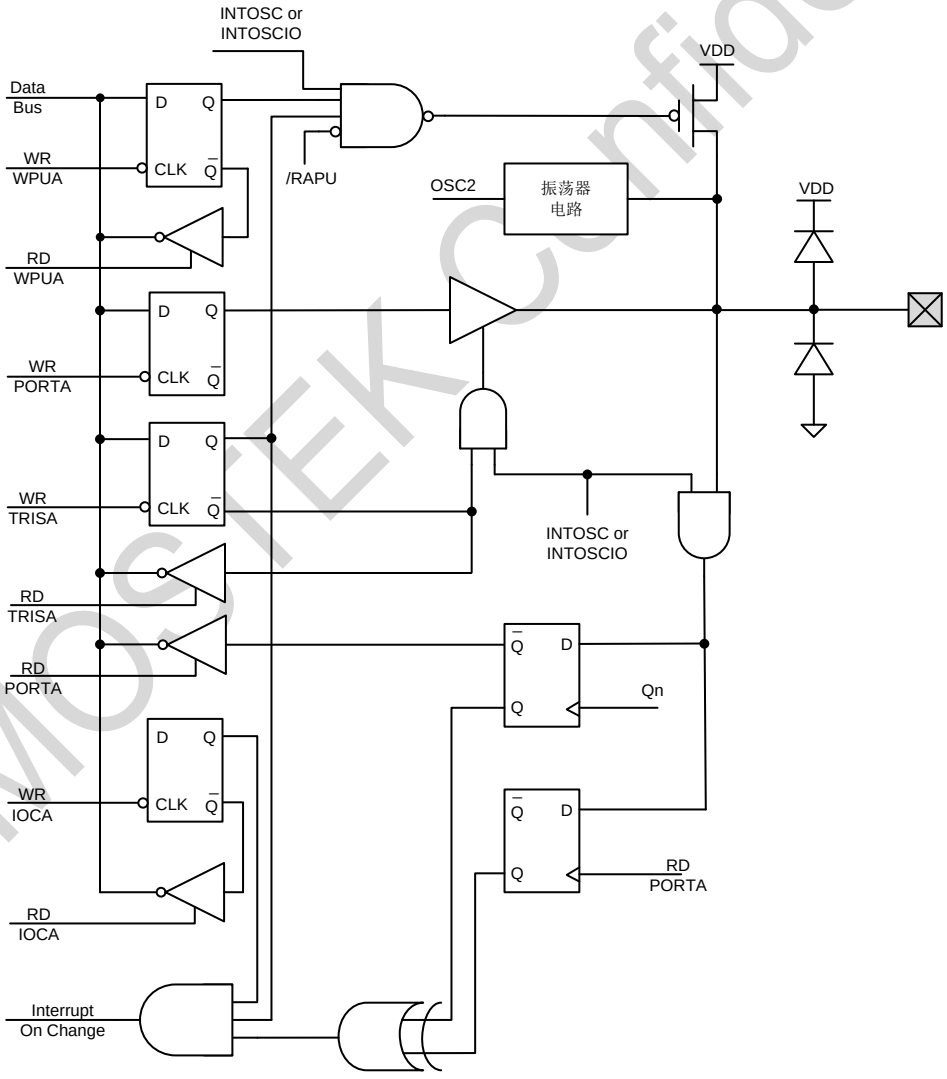


Figure 32. PA7 Architecture

16.3.6 PORTC<7:0>

PC7~PC0 can be configured as the following functional port:

- GPIO
- RFDIN, the data input in the RF pass-through mode (for PC0 only)
- SCLK, the the serial clock of the RF part SPI (for PC2 only)
- CSB, the chip selection of RF part SPI (for PC3 only)
- SDIO, the serial data of RF part SPI (for PC4 only)
- Comparator input (for PC0 and PC1 only, however it is not available since the ports are used to control the RF part)
- Comparator output (for PC4 only, however it is not available since the port are used to control the RF part)

The internal circuit architecture of the port is shown in the below figure.

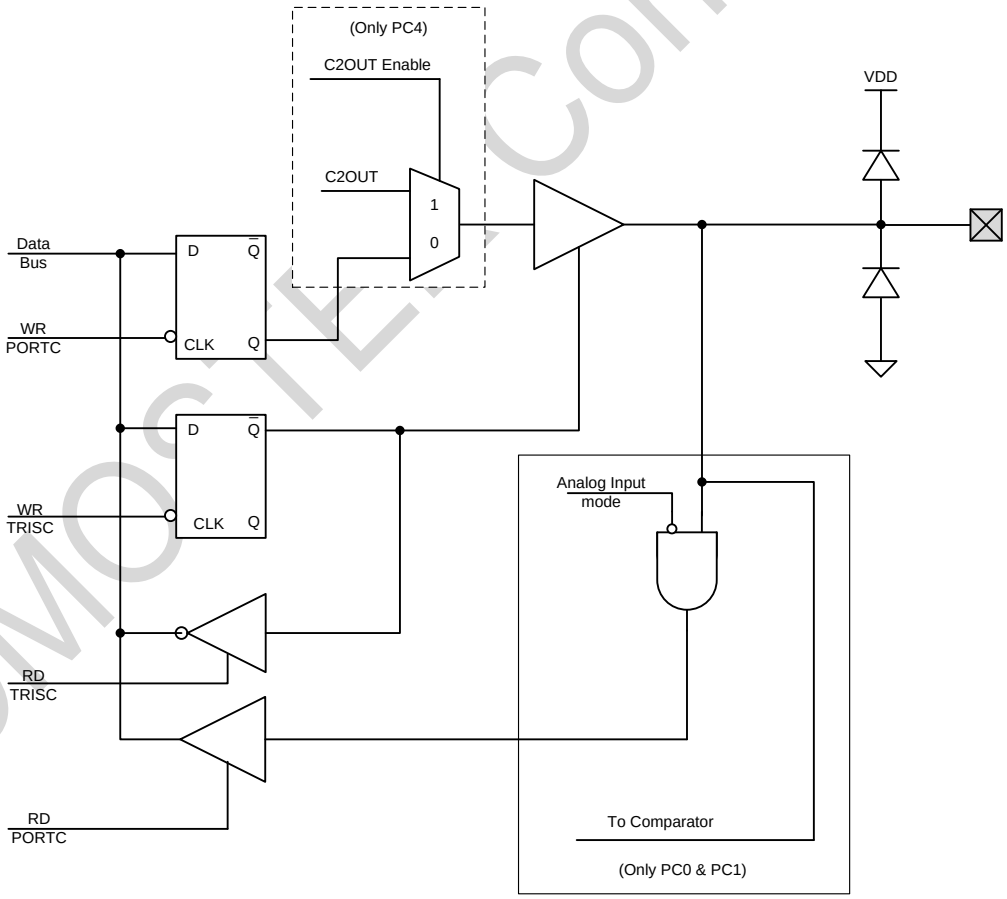


Figure 33. PC7~PC0 Architecture

17 Instruction Set

The CMT2189B adopts the reduced instruction set architecture with a total of 37 instructions. The instruction description is listed in the below table..

Table 90. Instruction Set Table

CMD	Instruction Period	Function	Operation	Status
BCR R, b	1	Bit clear	0-> R(b)	NONE
BSR R, b	1	Bit set	1-> R(b)	NONE
BTSC R, b	1（2）	Bit test, skip if 0	Skip if R(b)=0	NONE
BTSS R, b	1（2）	Bit test, skip if 1	Skip if R(b)=1	NONE
NOP	1	No operation	None	NONE
CLRWDT	1	Clear WDT	0-> WDT	/PF, /TF
SLEEP	1	ENTER SLEEPMODE	0-> WDT, STOP OSC	/PF, /TF
STTMD	1	Store W TO TMODE	W-> TMODE	NONE
CTLIO R	1	Control IO direction reg	W-> IODIRr	NONE
STR R	1	Store W to reg	W-> R	NONE
LDR R, d	1	Load reg to d	R-> d	Z
SWAPR R,d	1	Swap halves reg	[R(0-3)R(4-7)]-> d	NONE
INCR R, d	1	Increment reg	R+ 1-> d	Z
INCRSZ R, d	1（2）	Increment reg, skip if 0	R+ 1-> d	NONE
ADDWR R, d	1	Add W and reg	W+ R-> d	C, HC, Z
SUBWR R, d	1	Sub W from reg	R- W-> d R+ /W+ 1-> d	C, HC, Z
DECR R, d	1	Decrement reg	R- 1-> d	Z
DECRSZ R, d	1（2）	Decrement reg, skip if 0	R- 1-> d	NONE
ANDWR R, d	1	AND W and reg	R& W-> d	Z
IORWR R, d	1	Inclu.OR W and reg	W| R-> d	Z
XORWR R, d	1	Exclu.OR W and reg	W^ R-> d	Z
COMR R, d	1	Complement reg	/R-> d	Z
RRR R, d	1	Rotate right reg	R(n)-> R(n-1), C-> R(7), R(0)-> C	C
RLR R, d	1	Rotate left reg	R(n)-> R(n+1), C-> R(0), R(7)-> C	C
CLRW	1	Clear working reg	0-> W	Z
CLRR R	1	Clear reg	0-> R	Z
RETI	2	Return from interrupt	Stack-> PC,1-> GIE	NONE
RET	2	Return from subroutine	Stack-> PC	NONE
LCALL N	2	Long CALL subroutine	N-> PC, PC+1-> Stack	NONE
LJUMP N	2	Long JUMP address	N-> PC	NONE
LDWI I	1	Load immediate to W	I-> W	NONE
ANDWI I	1	AND W and imm	W& I-> W	Z
IORWI I	1	Inclu.OR W and imm	W| I-> W	Z
XORWI I	1	Exclu.OR W and imm	W^ I-> W	Z

CMD	Instruction Period	Function	Operation	Status
R E T W I	2	Return, place imm to W	Stack-> PC, I-> W	NONE
A D D W I I	1	Add imm to W	W+I-> W	C, HC, Z
S U B W I I	1	Subtract W from imm	I-W-> W	C, HC, Z

Notes:

1. The TMODE register of the chip refers to the OPTION, namely, the operation of the STTMD instruction is to save W to OPTION.

18 Revise History

Table 91. Revise History Records

Version No.	Chapter	Description	Date
1.0	All	Initial release	2017-11-23
1.1	2	Increase the Section 2.7.1 'Tx rate description'	2017-11-29
1.2	All	'PC4/RFDIN"is modified as"PC0/RFDIN'	2018-01-09
1.3	4.1.14, 4.1.30	Update the function description of SLVREN bit. Change LVDEN to LVREN.	2018-12-19
1.4	All	Rewrite the whole EN version document	2019-03-29
1.5	2.9.2	Change Tx. process	2019-11-05

19 Contacts

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