CMT2219B Operation Guide for Special Features

Overview

This document mainly discusses the special features of the CMT2219B to guide users' design and application. It provides the RFPDK related configuration UI screenshots and the corresponding register information.

The product models covered in this document are shown in the table below.

Table 1. Product Models Covered in This Document

Product Model	Frequency Range	Modulation Method	Chip Function	Configuration Method	Package
CMT2219B	127 - 1020 MHz	(G)FSK/OOK	Receiving	Register	QFN16

Before reading this document, it is recommended to read the *AN161-CMT2219B Quick Start Guide* to understand the basic information of the product.

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1 CMT2219B Special Feature Settings

The corresponding RFPDK screen and settings of special features are shown in the below figure.

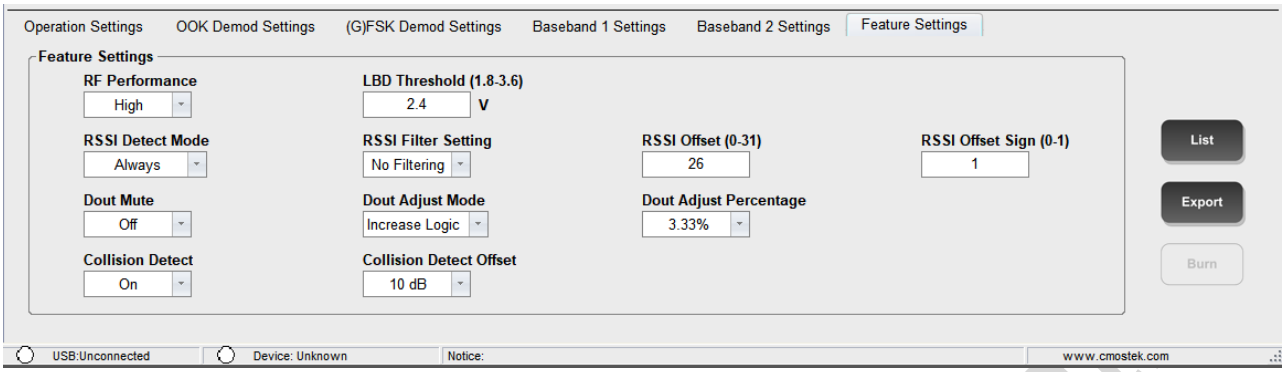

Figure 1. Special Feature Setting Screen

Table 2. Parameters for Special Feature

RFPDK Parameter	Register Bits
Dout Mute	DOUT_MUTE
Dout Adjust Mode	DOUT_ADJUST_EN
Dout Adjust Mode	DOUT_ADJUST_MODE
Dout Adjust Percentage	DOUT_ADJUST_SEL<2:0>
Collision Detect	COL_DET_EN
Collision Detect Offset	COL_OFS_SEL
RF Performance	LMT_VTR<1:0> MIXER_BIAS<1:0> LNA_MODE<1:0> LNA_BIAS<1:0>
LBD Threshold	LBD_TH<7:0>

1.1 FSK Demodulation Output Mute

The mute function means that, in Rx state, when there's no signal, the chip's demodulation output is always *0* without *0/1* reverse caused the fluctuations in the bottom noise. Once a signal appears, it outputs as usual without impact of mute. The advantage of the mute function is that, when demodulation output is used as waking-up input, MCU will never be woken-up if there's no signal,.

The mute function only works in direct mode, in which the demodulated data is configured to output to GPIO directly, then sampled and decoded by MCU.

In FSK mode, the mute function is implemented by the phase jump detection (PJD) mechanism discussed in the chapters for channel listening. Users need to configure a register to enable the FSK mute function.

Table 3. FSK Demodulation Output Mute

Register	Bit	R/W	Flag	Description
CUS_SYS10 (0x15)	4	RW	DOUT_MUTE	This register is applicable to FSK mode. Mute function enabling. 0: disable 1: enable

The task of PJD is to identify useful signals and noise, and give indication when a useful signal appears. This indication can be used for mute enabling control.

1.2 Adjustment to Duty Cycle of Demodulation Output

The registers below are used to adjust the duty cycle of 1 and 0 of the demodulation output. These registers are shared by OOK and FSK.

Table 4. Adjustment to Duty Cycle of Demodulation Output

Name	Bit	R/W	Flag	Description
CUS_CDR2 (0x2C)	4:2	RW	DOUT_ADJUST_SEL<2:0>	The adjustment percentage of duty cycle. 0：3.33% 1：6.66% 2：9.99% 3：13.32% 4：16.65% 5：19.98% 6：23.21% 7：26.64%
	1	RW	DOUT_ADJUST_MODE	Adjusting the direction of duty cycle. 0: increase the duty cycle of 1 1: decrease the duty cycle of 1
	0	RW	DOUT_ADJUST_EN	Demodulation output duty cycle adjustment enabling. 0: disable 1: enable

The duty cycle adjustment is based on data *1*. If a data preamble (with a pattern of 10101010) is received, assuming the original duty cycle is 50-50, to increase the duty cycle of *1* by 3.33%, it makes the duty ratio of all *1* become 53.33% and the duty ratio of all *0* become 46.67%. The adjusting principle for non-preamble data (the length of *1* and *0* is not fixed) is just the same, that is, it increases the length of the successive data *1* by 3.33% symbols and decreases the length of the following successive data *0* by 3.33% symbols, no matter how many symbols of *1* or *0* contained in each group of successive data *1* or *0*.

1.3 Signal Collision Detection

In environments where the in-band interference is large and frequent, collision detection can help the MCU identify the error packets in advance, saving MCU from the time-consuming work of verifying the wrong data. The registers related to conflict detection are listed in the below table.

Table 5. Signal Collision Detection

Register	Bit	R/W	Flag	Description
CUS_SYS10 (0x63)	7	RW	COL_DET_EN	Signal collision detection enabling. 0: disable 1: enable
	6	RW	COL_OFS_SEL	Threshold for determination of signal collision. 0: 10 dB 1: 16 dB

The CMT2219B supports a simple method for channel collision detection. For example, when receiving a data packet, the receiver detects a preamble followed by sync word, however a further preamble is received, which is suspicious (a preamble should not appear after sync word in normal case). The chip then detects the RSSI of the suspect preamble and compares it with the RSSI of the previously received preamble. If the suspect RSSI is 10 dB or 16 dB (selected by COL_OFS_SEL) greater than the valid RSSI, the suspect one is determined as in-band interference. As its RSSI is much larger than that of the valid data packet received currently, it must have interfered with the currently received data, therefore a COL_ERR interrupt is output to the MCU for further processing.

If the RSSI difference between two successive preambles is less than a threshold, it means that the suspect preamble currently received actually is part of the valid data packet with some part of the data same with the valid preamble. However its RSSI suddenly changes a little under some conditions such as the distance change between the transmitter and the receiver. In other cases, it is interference really, however its RSSI is 3+ dB less than that of the valid data packet, therefore it will not affect valid data packets receiving, other words, it can be ignored.

The PKT_DONE interrupt will be generated and output to MCU based on the result of logic OR operation on the COL_ERR interrupt source, PKT_ERR and PKT_OK. Once receiving this interrupt, the MCU queries the bit flag first to determine the interrupt source. If the interrupt source is COL_ERR, the FIFO data currently being received can be discarded because it is known to have been interfered with thus the data is definitely wrong. After then, it exits Rx and re-enter it again for data receiving. This way, the MCU does not have to wait until all the data packets have been received to know the original data is in error, thus it has the advantage of saving both energy and time by the processing in advance.

1.4 RF Current Adjustment to Receiver

The CMT2219B provides a set of registers for users to reduce the RF current of receiver, however the performance will be declined accordingly. The relevant registers are listed in the below table.

Table 6. RF Current Adjustment to Receiver

Register	Bit	R/W	Flag	Description
CUS_SYS1 (0x0C)	7:6	RW	LMT_VTR<1:0>	The current level of LMT VTR.
	5:4	RW	MIXER_BIAS<1:0>	The current level of mixer.
	3:2	RW	LNA_MODE<1:0>	The current level 1 of LNA.
	1:0	RW	LNA_BIAS<1:0>	The current level 2 of LNA.

Reducing the current will cost the RF performance declining correspondingly. The configuration methods of the 4 registers are shown in the below table.

Table 7. Configuration Methods of Current Register

Current Level	RF Performance Level	LMT_VTR<1:0>	MIXER_BIAS<1:0>	LNA_MODE<1:0>	LNA_BIAS<1:0>
Low	Low	2	2	1	1
Medium	Medium	2	2	1	2
High	High	1	2	3	2

1.5 Low Battery Detection (LBD)

The CMT2219B supports LBD function. The related registers are listed in the below table.

Table 8. Low Battery Detection - Register in Configuration Area

Register	Bit	R/W	Flag	Description
CUS_SYS10 (0x63)	7	RW	LBD_TH<7:0>	The LBD threshold for compare.

Table 9. Low Battery Detection - Register in Control Area

Register	Bit	R/W	Flag	Description
CUS_LBD_RESULT (0x71)	7	RW	LBD_RESULT<7:0>	LBD detection result.

The LBD principle is that, based on the LBD_TH (the threshold of LBD) set by users, it calculates according to the below formula.

VTH = LBD_TH / 255 X 4.8 V

Then, while performing LBD, the chip measures the voltage of VDD and converts it to LBD_RESULT according to the similar formula below.

VDD = LBD_RESULT / 255 X 4.8 V

After then, when obtaining the measurement result, the chip compares LBD_RESULT with LBD_TH. If LBD_RESULT is smaller than LBD_TH, meaning that the low voltage has already occurred, the LBD interrupt will be output to notify the external MCU for further processing. It is recommended that the MCU clears this interrupt immediately before proceeding further. Besides, the LBD processing of the CMT2219B is not in real time, with no specific command for it. It performs LBD once while the PLL is doing frequency correction, which is performed during switching from SLEEP/STBY to RFS//RX.

2 Revise History

Table 10. Revise History Records

Version No.	Chapter	Description	Date
0.7	All	Initial version	2018-10-10

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